

Compal LA-L973P

HH514(50) MB Schematic Document

Rev : 1.0

2021.10.26

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**mDP - JDP1**  
- VGA Port A  
Reserve  
P. 41

**HDMI - JHDMI1**  
- VGA Port C  
HDMI  
P. 40

**GN20P**  
- GDDR6 4G  
Note:  
GN20 support PCIe Gen4 only  
P. 27-37

**eDP - JEDP1**  
- CPU eDP  
P. 38

DDIA

PEG x8  
8/32GT/s

**Intel Alder Lake-P H45 Processor**

Memory BUS

**Interleaved (DDR4)**  
- DDR4 So-DIMM 260 pin  
- Channel A  
P. 23  
- DDR4 So-DIMM 260 pin  
- Channel B  
P. 24

**VBIOS ROM**  
- SOP8  
- Size : 2M  
P. 29

**LAN(GbE) JRJ45**  
- PCIe 1.0 2.5GT/s  
- Port 12  
- E2600  
P. 73

**USB3.1 - JUSB 3**  
- GEN1  
- USB3.1 Port 3  
- USB2.0 Port 4  
P. 73

**USB3.1 - JUSB 2**  
- GEN2  
- USB3.1 Port 2  
- USB2.0 Port 3  
P. 73

**USB3.1 - JUSB 1**  
- GEN2  
- USB3.1 Port 1  
- USB2.0 Port 2  
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**Type C (TBT4) - JTYPEC1**  
- USB-C TCP0  
- USB2 Port 1  
P. 42-43

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**SPI ROM 32M**  
- WSOP8  
- Size : 32M  
P. 16

eSPI BUS

P. 06-22

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- Port 11 (SATA 0)  
P. 67

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- PCIe4 Port B  
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**SSD - JSSD1 (PCIe)**  
- PCIe4 Port A  
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DMIC

I2C

**Touch Pad**  
- EC PS2  
- PCH I2C1  
P. 63

**EC KB9542**  
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I2C/PS2

Fan Control\*2  
page 77

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- PCIe Port 4  
P. 52

**CCD Camera**  
- Port 6  
P. 38

**Finger print**  
- USB2 Port 7  
P. 66

**Per key**  
- USB2 Port 8  
P. 38

**HDA Codec**  
- AL3324  
P. 56

**Int. Speaker**  
- ON M/B > L  
- ON M/B > R

**Audio Jack**  
- On IO/B

**Int. DMIC**  
- On CCD Module

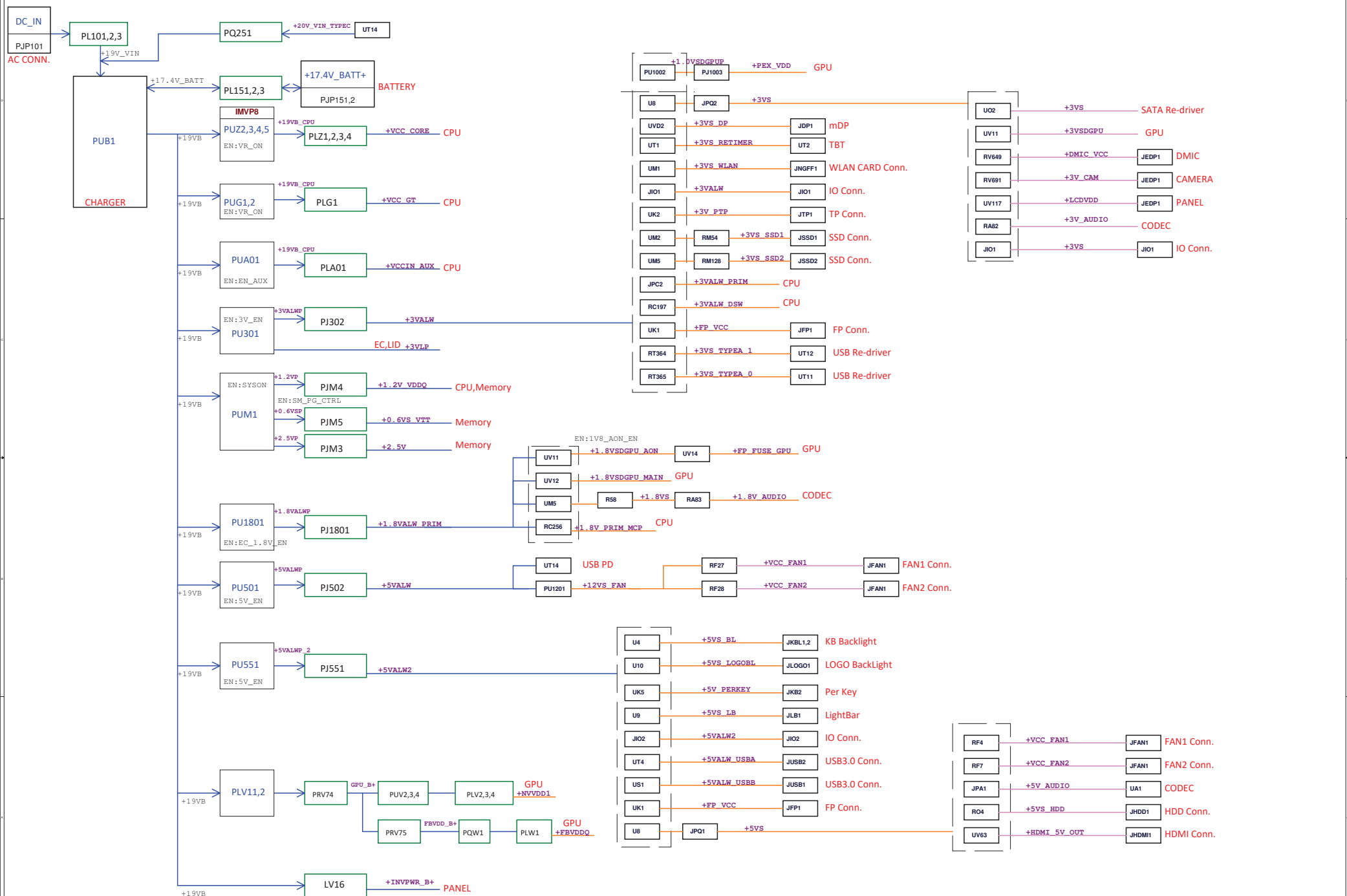
**Int.KBD**  
- KSI/KSO  
- Single RGB  
(32pin + 6pin)  
P. 63

**Sub Board**

IO/B (JIO1/JIO2)	P. 73
Turbo Key/B (JTRB1)	P. 77
RTC CKT. (JRTC1)	P. 20
Power On/Off CKT.	P. 63
HW Circuit DC/DC	P. 78
Power Circuit DC/DC	P. 81-118

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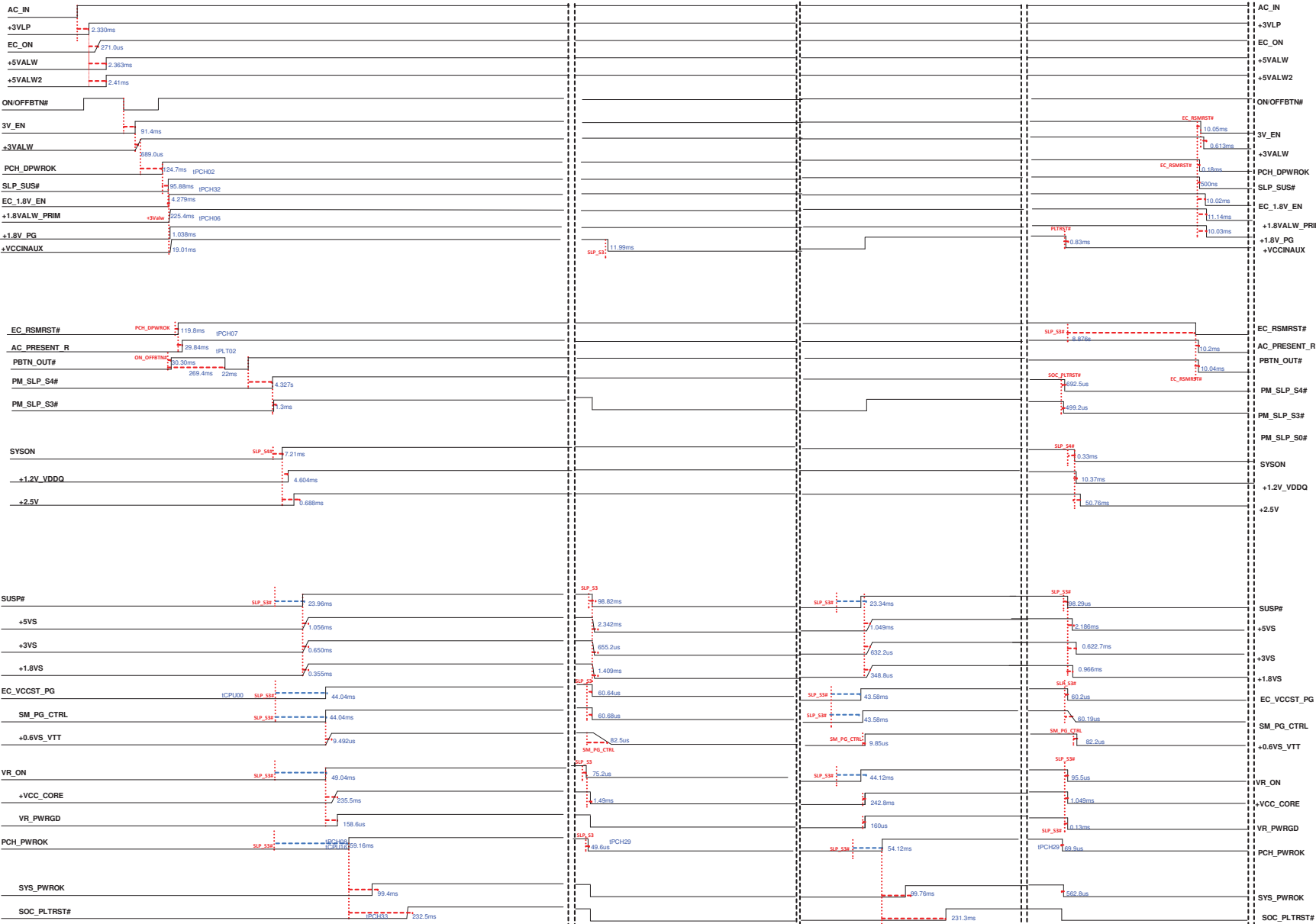


G3→S0

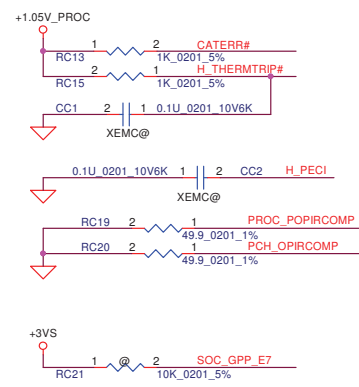
S0→S3

S3→S0

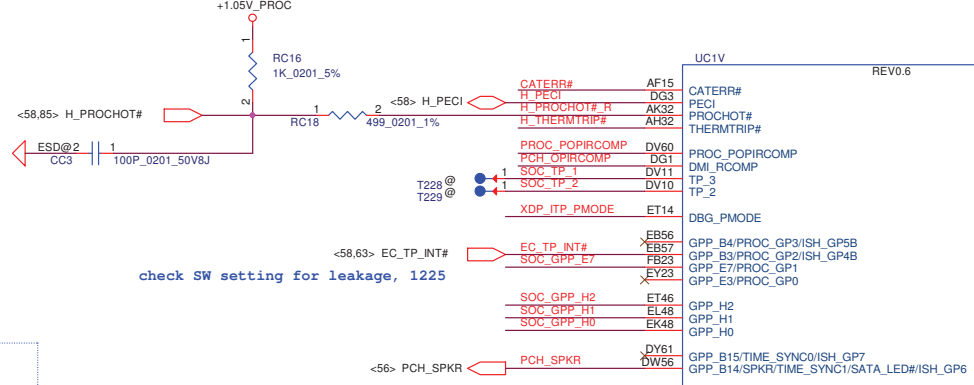
S0→S5



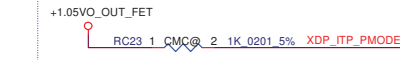




CHECK power net name, 05/17

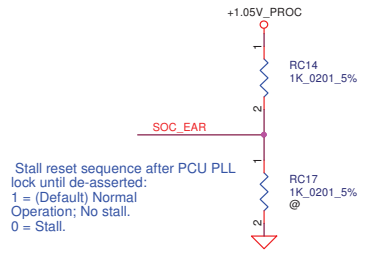
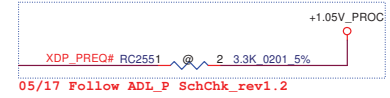
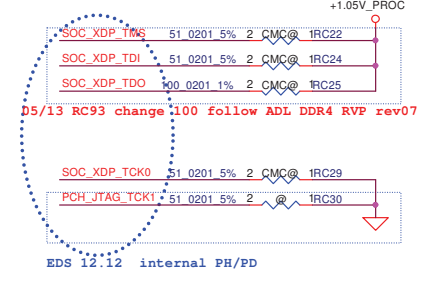
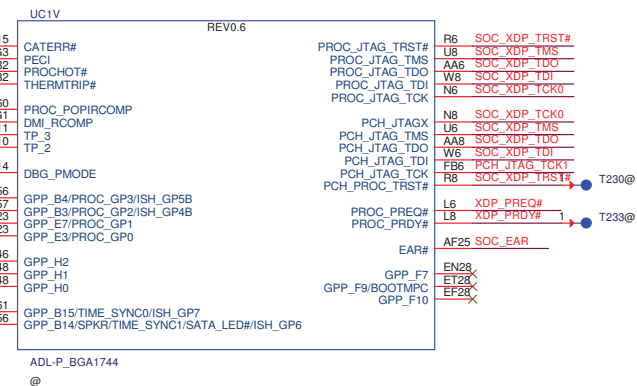
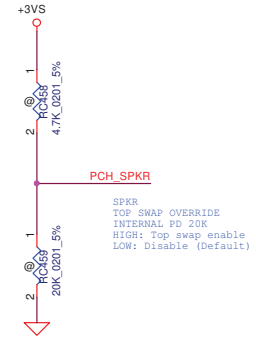


check SW setting, 1225



This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.

### Strap Pin

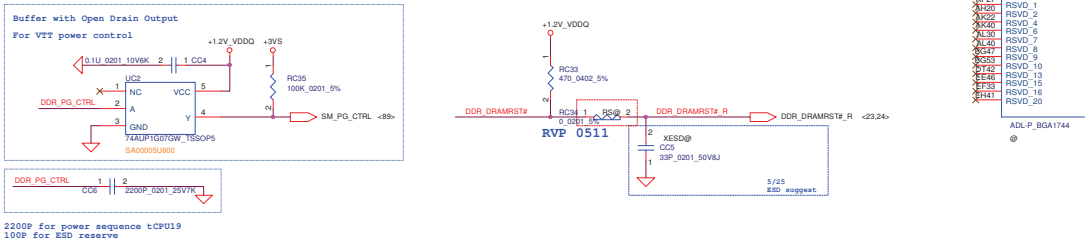
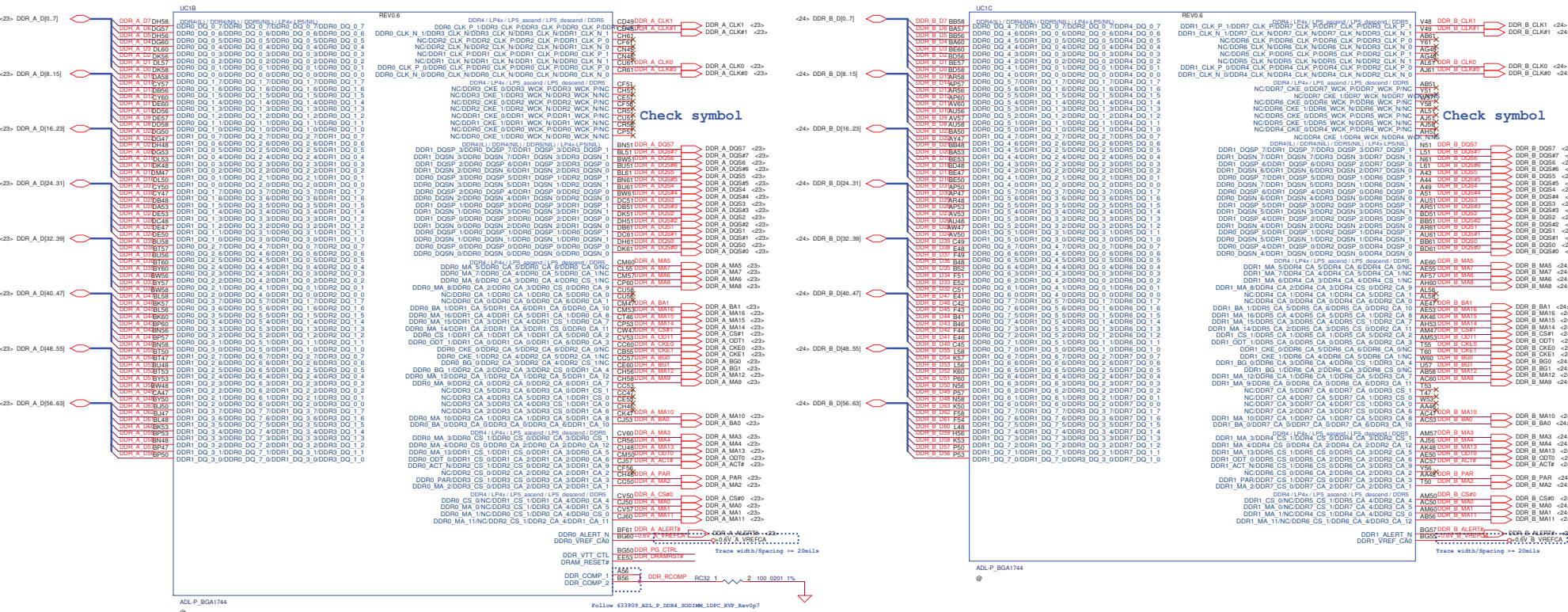


Stall reset sequence after PCU PLL lock until de-asserted:  
1 = (Default) Normal Operation; No stall.  
0 = Stall.

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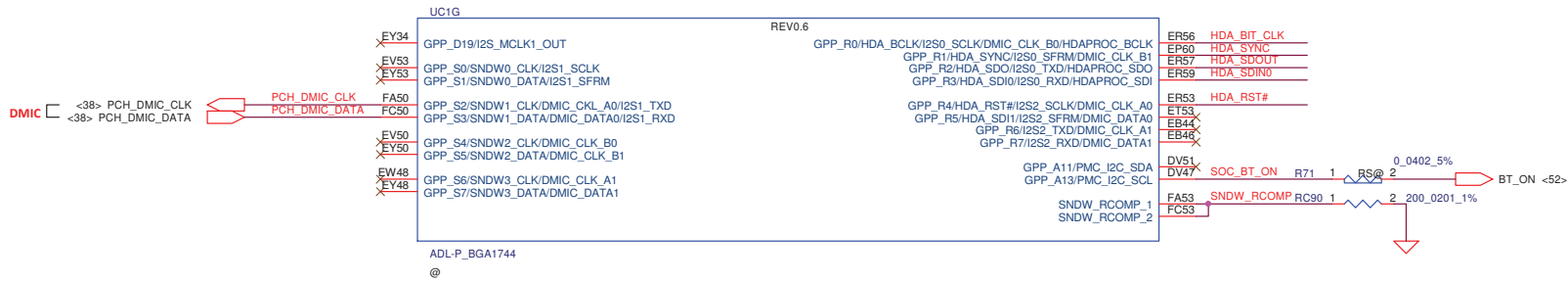
**Follow Intel DDR4 N1L**

DDR4: Refer to ADL\_P\_DDR4\_SODIMM\_1DPC\_RVP\_Rev0p7

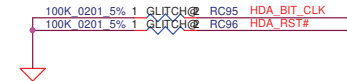
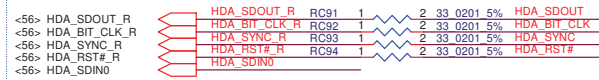




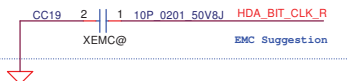




### HDA for AUDIO



Follow  
627205\_ADL\_P\_PDG for Glitch



### To Enable ME Override



572631\_ICL\_PCH\_IP\_EDS\_Vol\_1\_Rev\_0p7

VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V

Need to sync with codec VDDIO

HDA\_SDOOUT

FLASH\_DESCRIPTOR SECURITY OVERRIDE

INTERNAL PD 20K

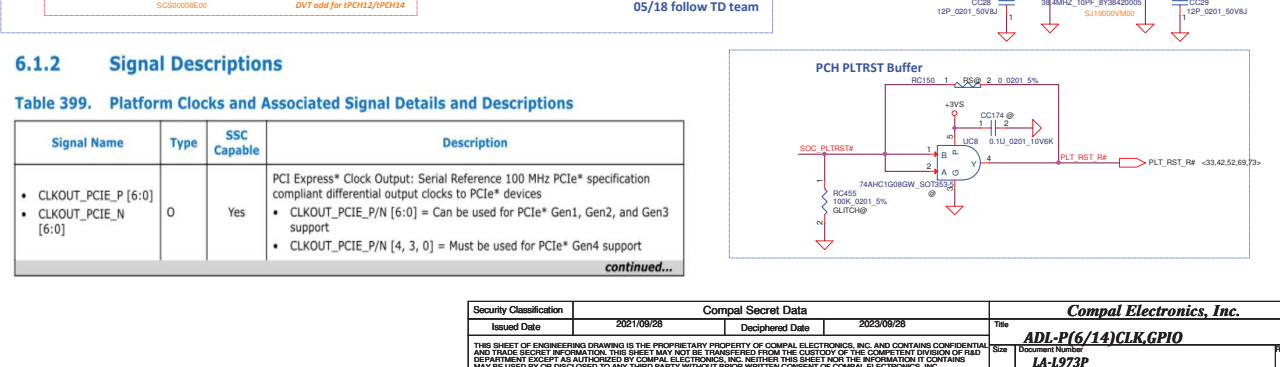
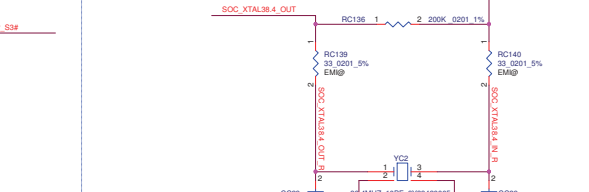
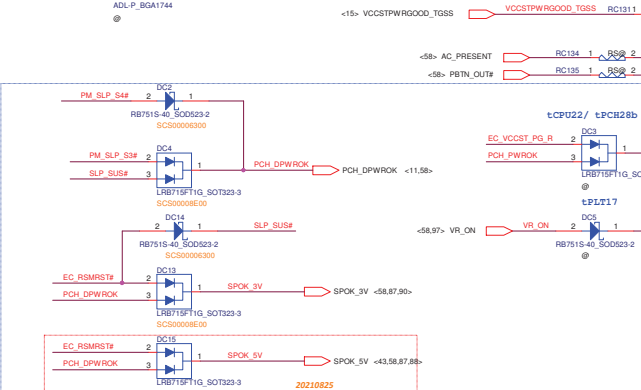
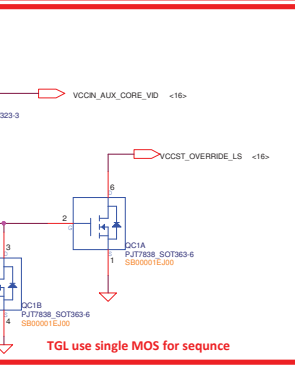
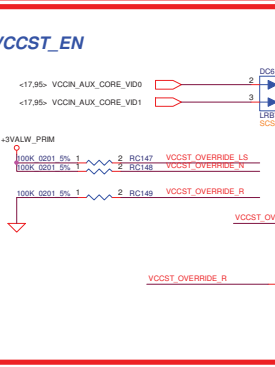
HIGH: OVERRIDEN

LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

HDA_SYNC	CC12	@RF@1	2	22P 0201 25V8
HDA_BIT_CLK	CC13	@RF@1	2	22P 0201 25V8
HDA_SDOOUT	CC14	@RF@1	2	22P 0201 25V8
HDA_SDIN0	CC15	@RF@1	2	22P 0201 25V8
HDA_RST#	CC16	@RF@1	2	22P 0201 25V8
PCH_DMIC_CLK	CC17	@RF@1	2	22P 0201 25V8
PCH_DMIC_DATA	CC18	@RF@1	2	22P 0201 25V8

Close SOC

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### 6.1.2 Signal Descriptions

**Table 399. Platform Clocks and Associated Signal Details and Descriptions**

Signal Name	Type	SSC Capable	Description
<ul style="list-style-type: none"> <li>CLKOUT_PCIE_P [6:0]</li> <li>CLKOUT_PCIE_N [6:0]</li> </ul>	0	Yes	PCI Express® Clock Output: Serial Reference 100 MHz PCIe® specification compliant differential output clocks to PCIe® devices <ul style="list-style-type: none"> <li>CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe® Gen1, Gen2, and Gen3 support</li> <li>CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe® Gen4 support</li> </ul>

*continued...*

*continued...*



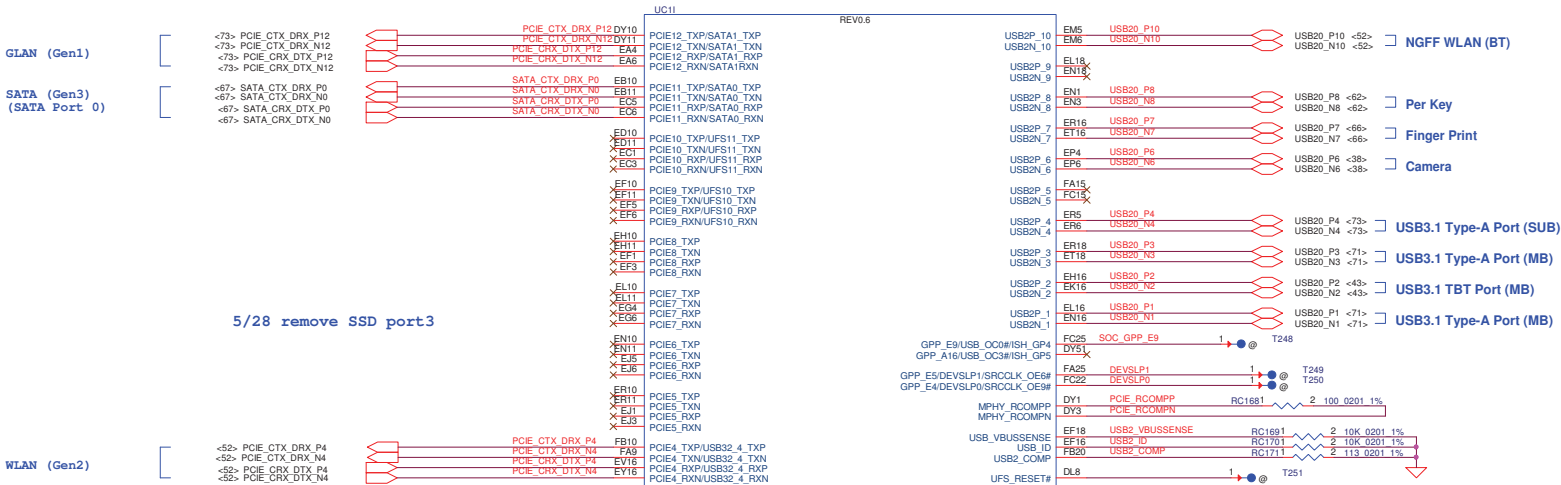
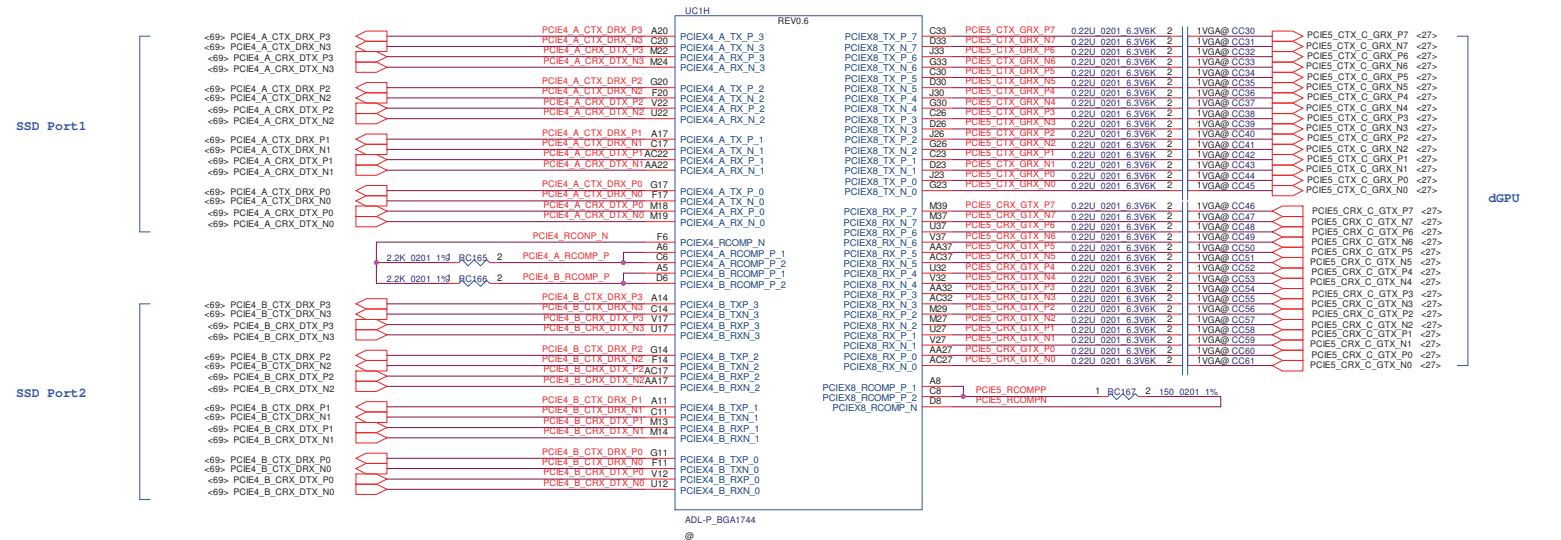
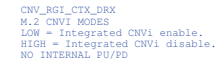


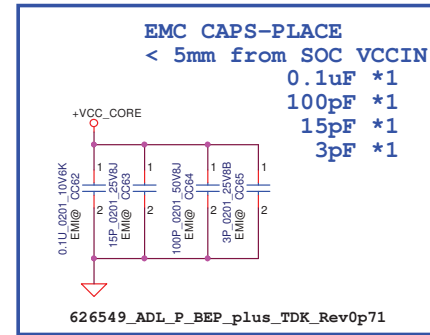
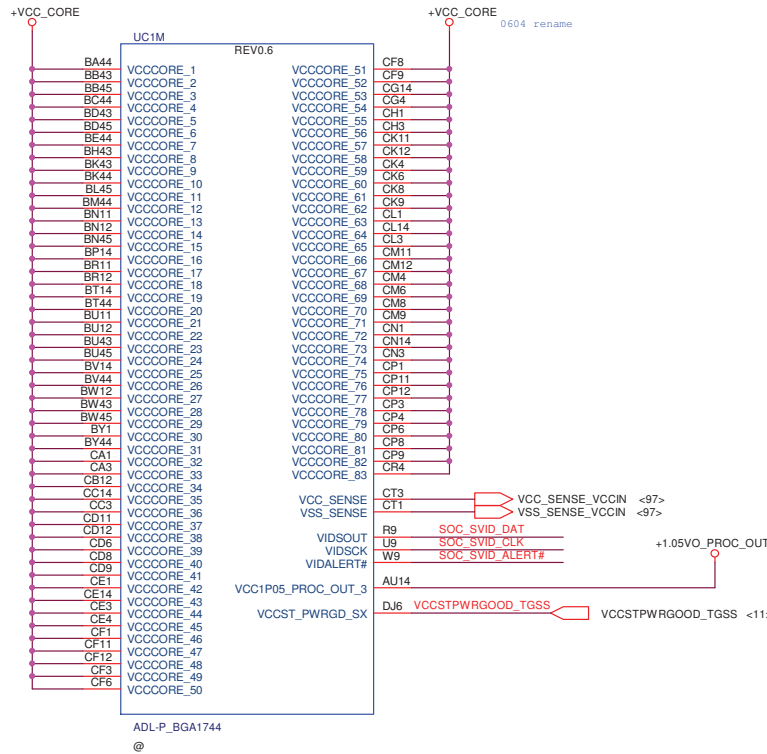
Table 180. USB3/USB2 Port Pairing for USB-C\* Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

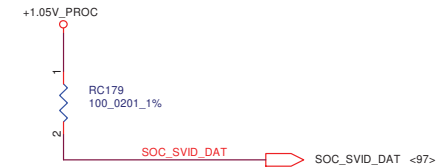
To make split xDCI controller working functionally for different USB-C\* connectors with increasing port numbers (TCP0\_\*, TCP1\_\*, TCP2\_\*, TCP3\_\*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C\* connectors, but it is not strictly required.



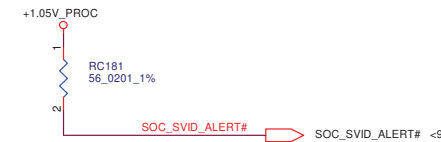
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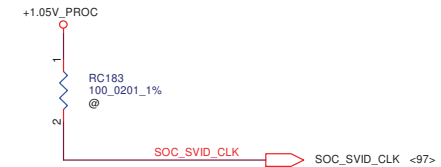
## SVID DATA



## SVID ALERT



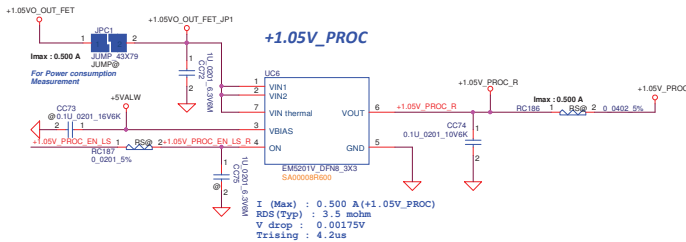
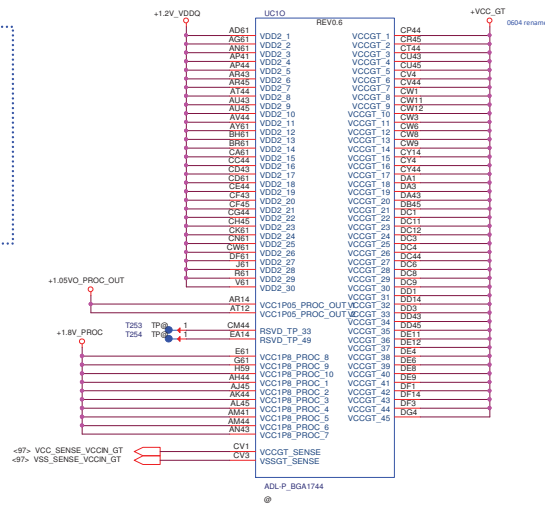
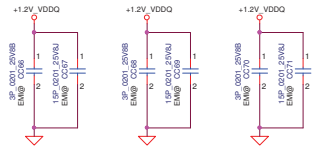
## SVID CLOCK



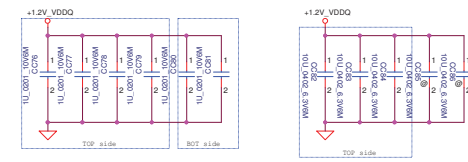
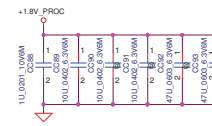
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627333\_ADL\_P\_DDR4\_RVP\_TDK\_Rev0p7

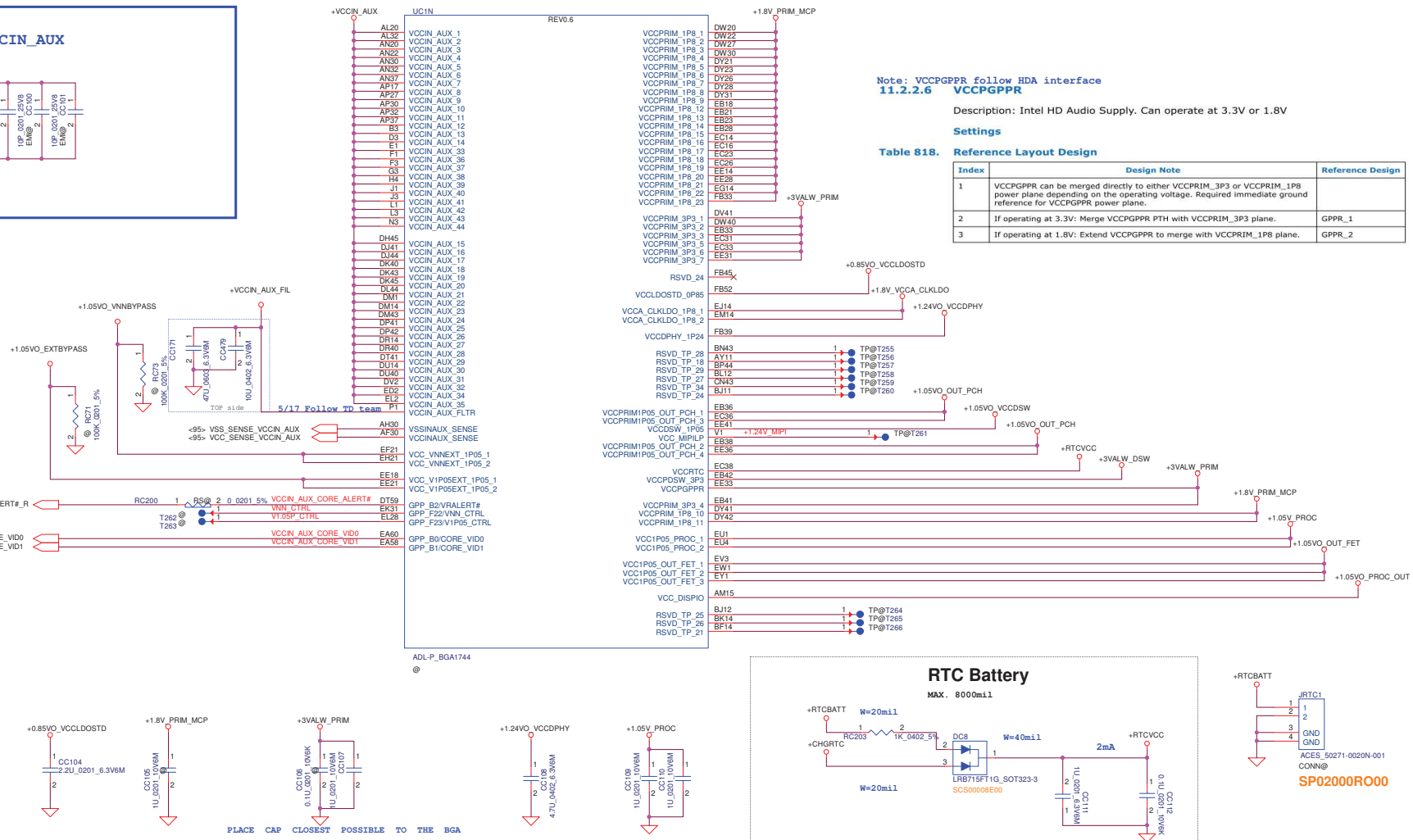
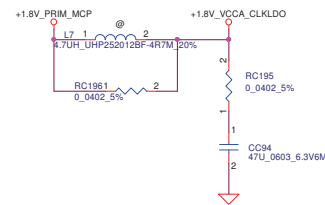
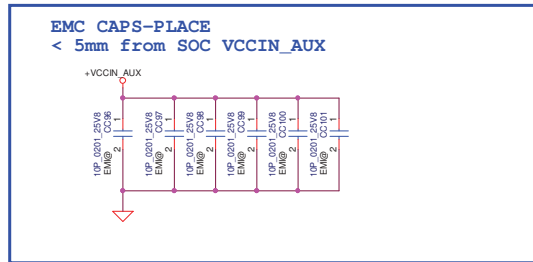
[illegible]

Sideband signals(PEC1,THERMTRIP,PROCHOT,VCCST\_PWRGD,SVID) should be connected to **VCC1P05\_PROC** rail when there is Power Gate or to **VCC1P05\_OUT\_FET** (which should be shorted to VCC1P05\_OUT\_FET)rail when there is no Power Gate.

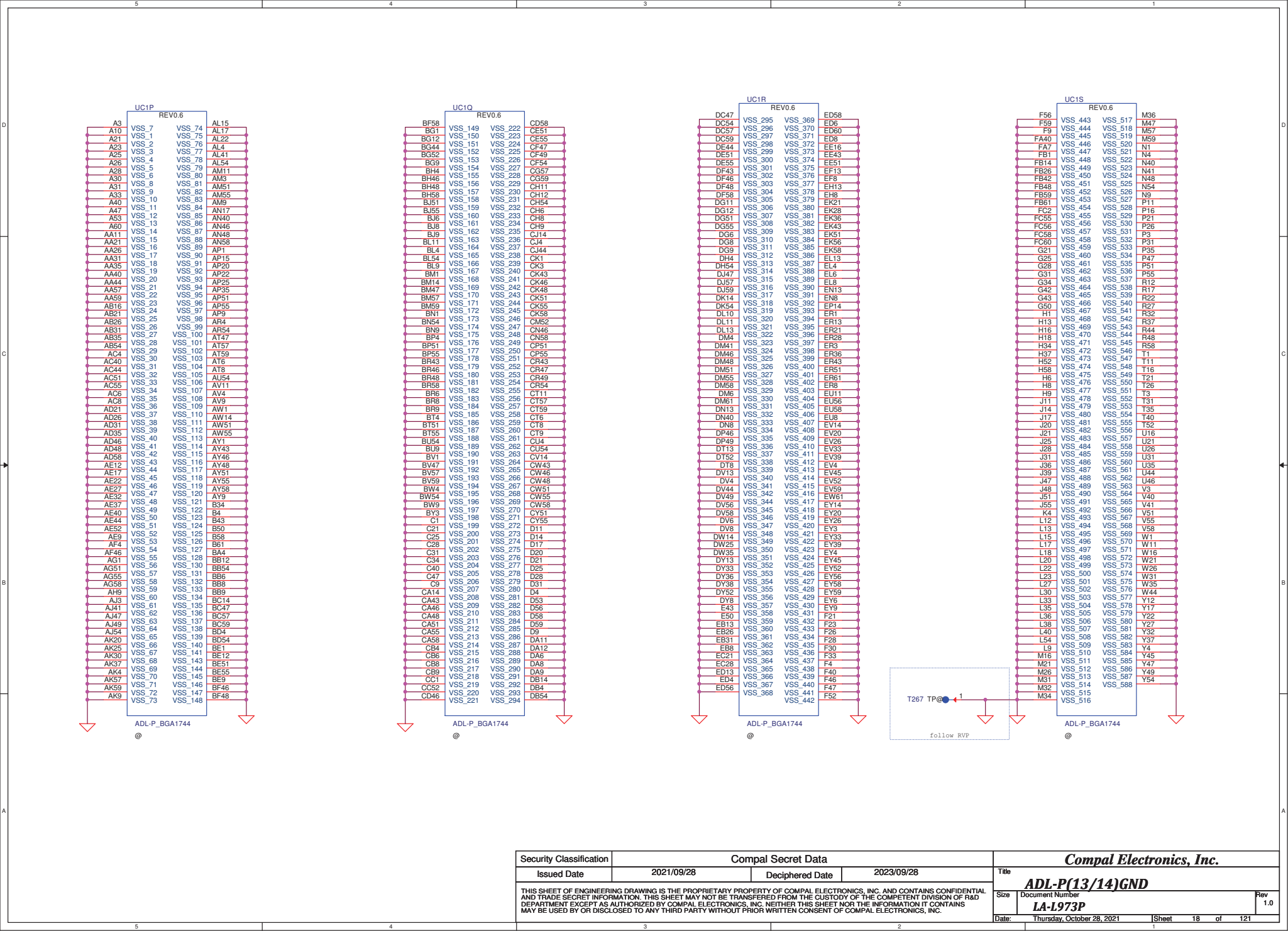


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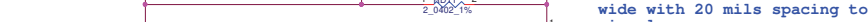
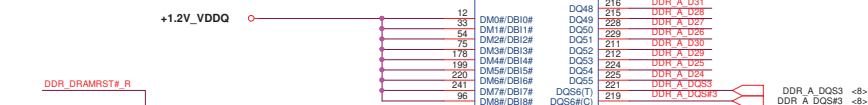
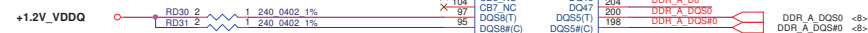
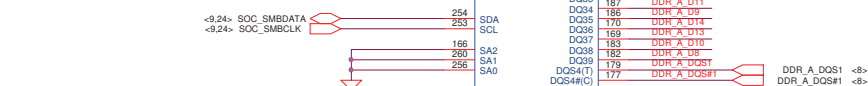
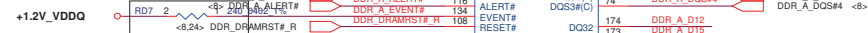
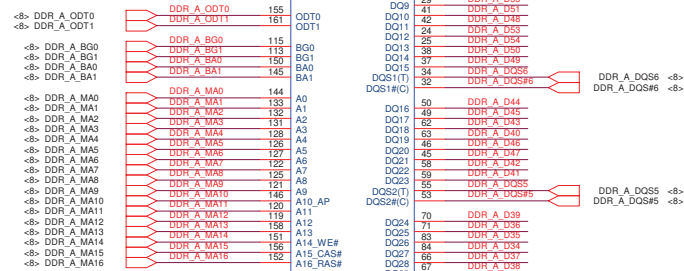
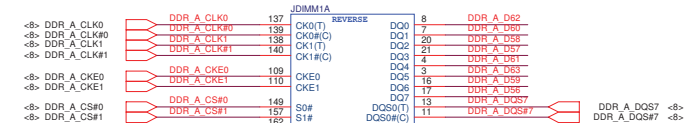
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# Reserve Page

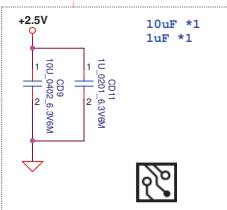
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				Document Number	1.0
				Date:	Thursday, October 28, 2021
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## > Non-ECC SO-DIMM



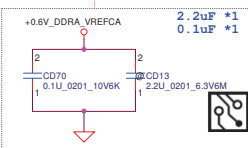
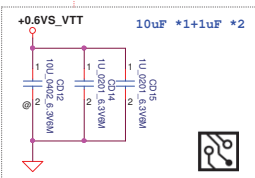
PLACE NEAR TO PIN

Layout Note:  
Place near JDIMM1B.257,259

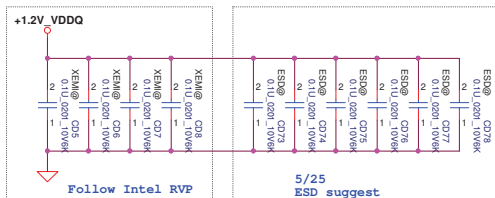


Layout Note:  
PLACE THE CAP near JDIMM1B. 164

Layout Note:  
Place near JDIMM1B.258

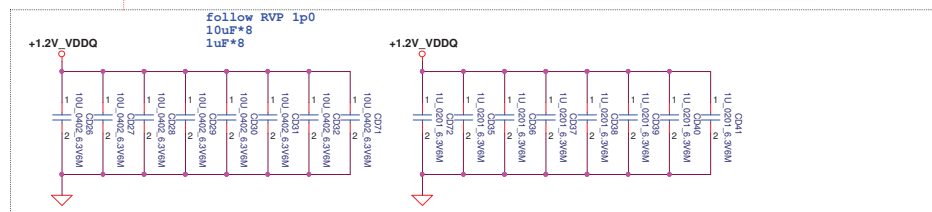


**Layout Note:**



Follow Intel

5/25  
ESD suggest



Part Number: SP07001CY00  
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4

PLACE NEAR TO SODIMM

### REFERENCES

+1.2V VDDQ

I Max = 3.44A  
2 channel -->  $3.44 / 2 = 1.72A$

## DIMM Side

## CPU Side

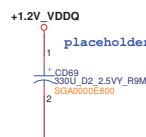
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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### > Non-ECC SO-DIMM



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



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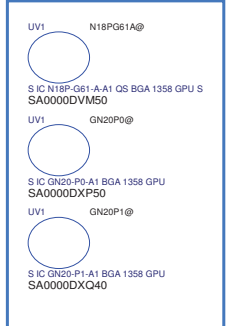
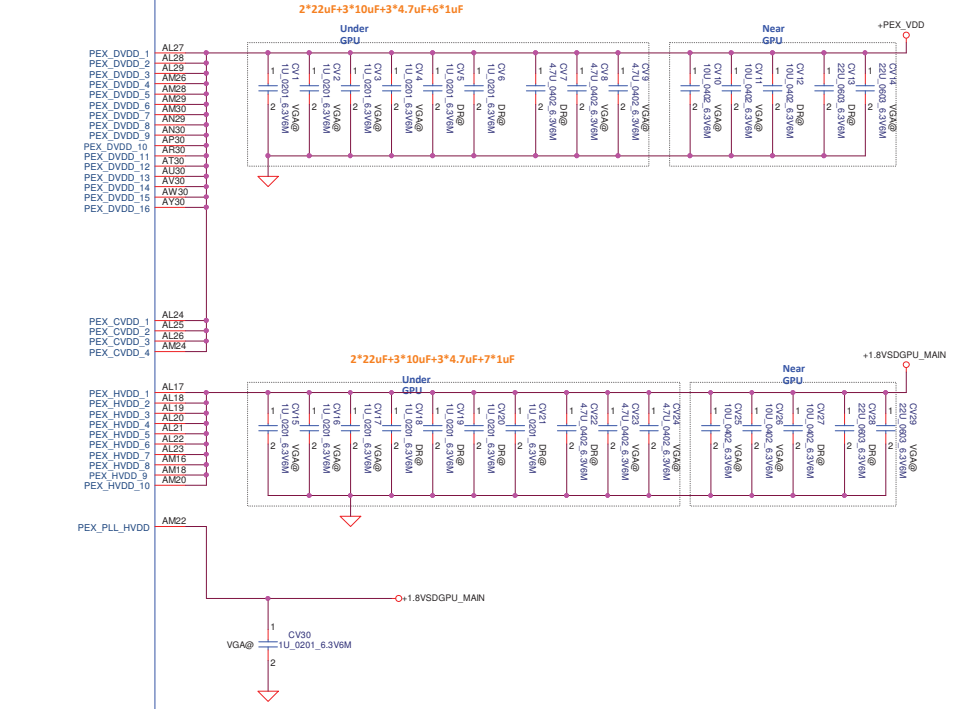
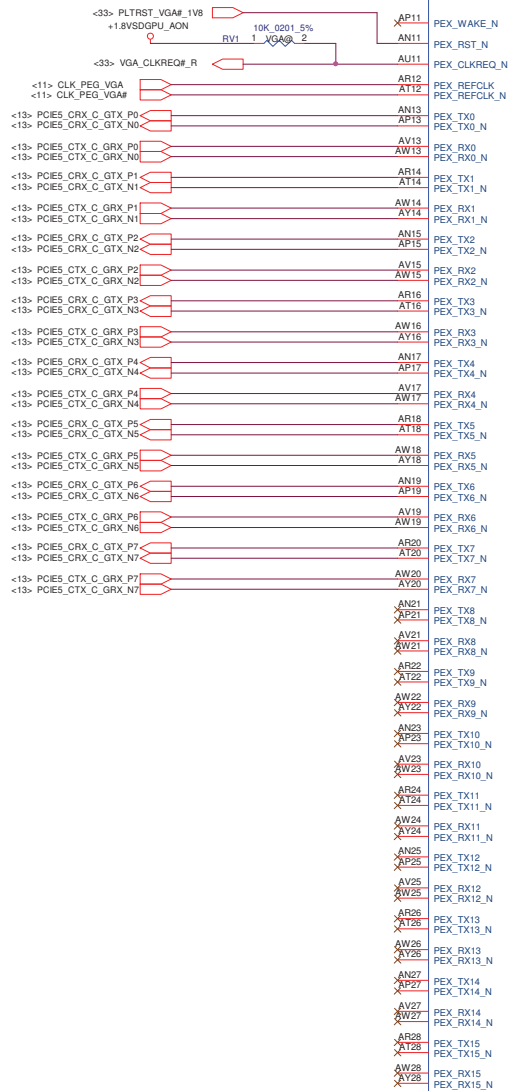
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				Date:	Thursday, October 28, 2021
				Sheet	25 of 121
				Rev	1.0

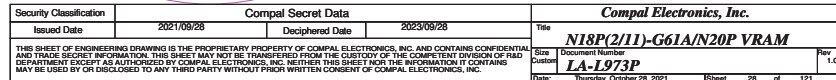
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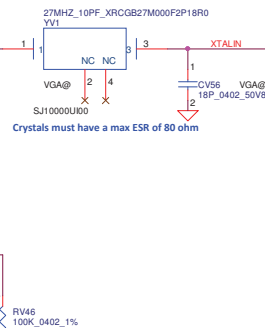
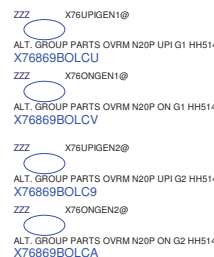
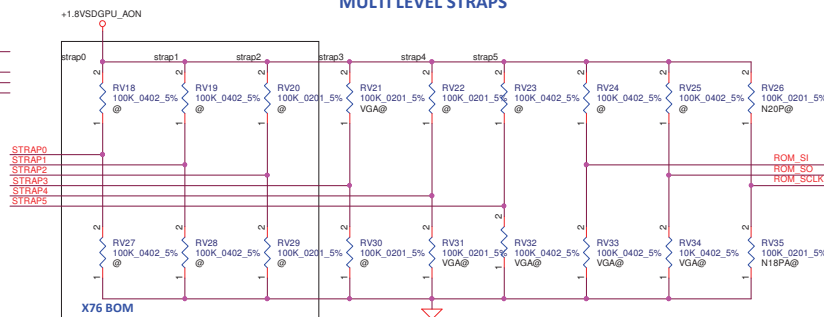
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				Date:	Thursday, October 28, 2021
				Sheet	26 of 121
				Rev	1.0

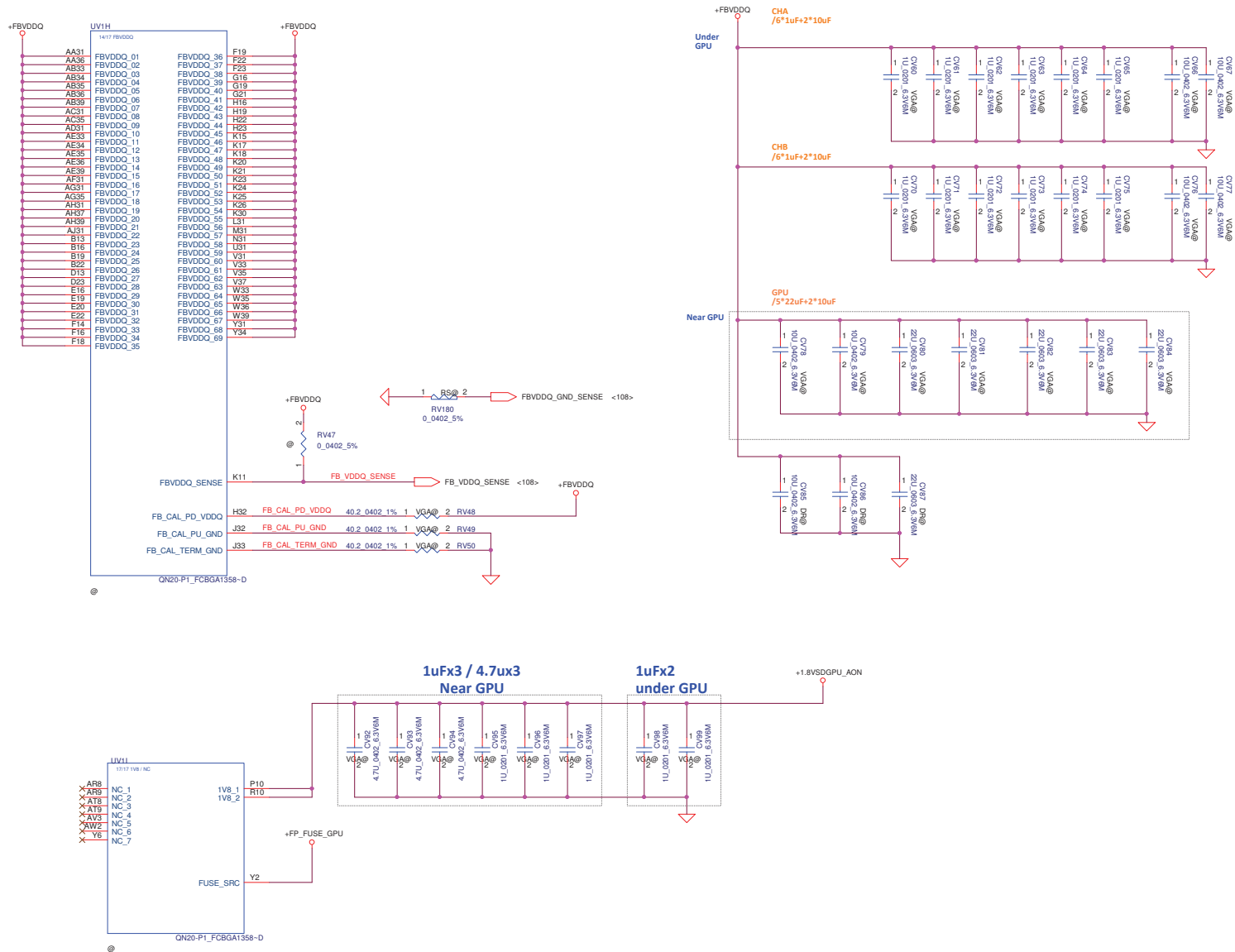
To N18PG61A / N20P DGPU x 8 Lane

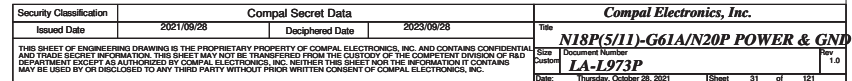


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Rev		1.0		LA-1973P							







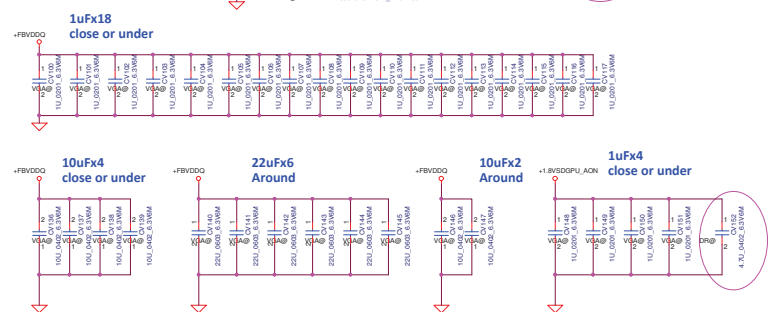
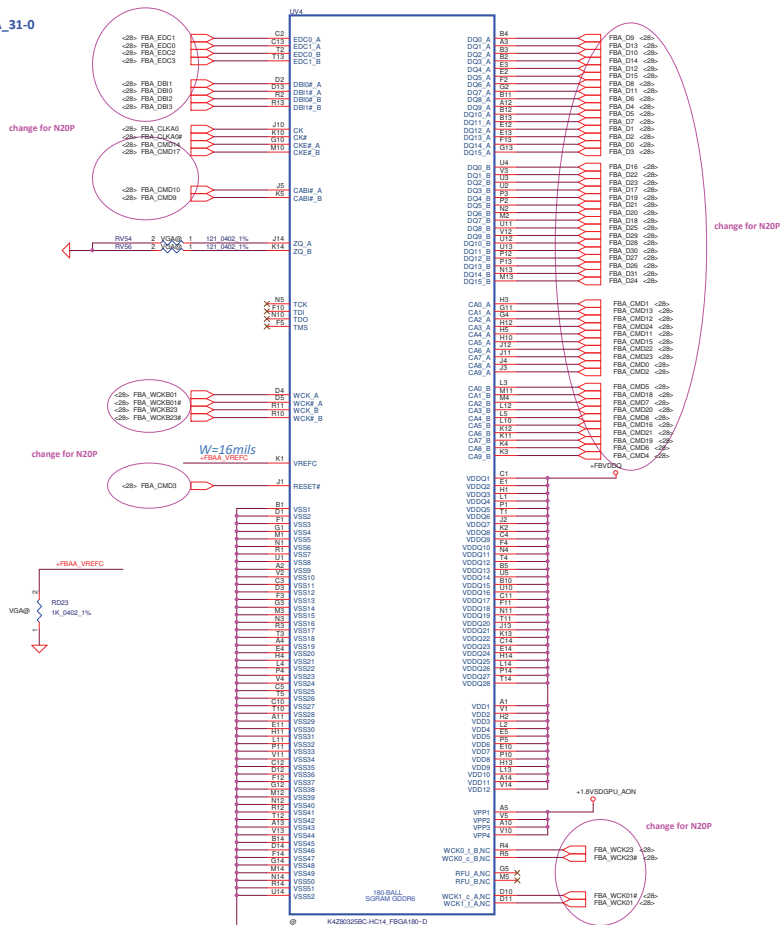




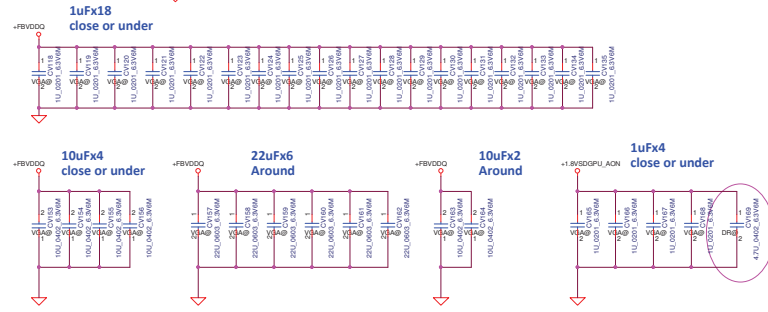
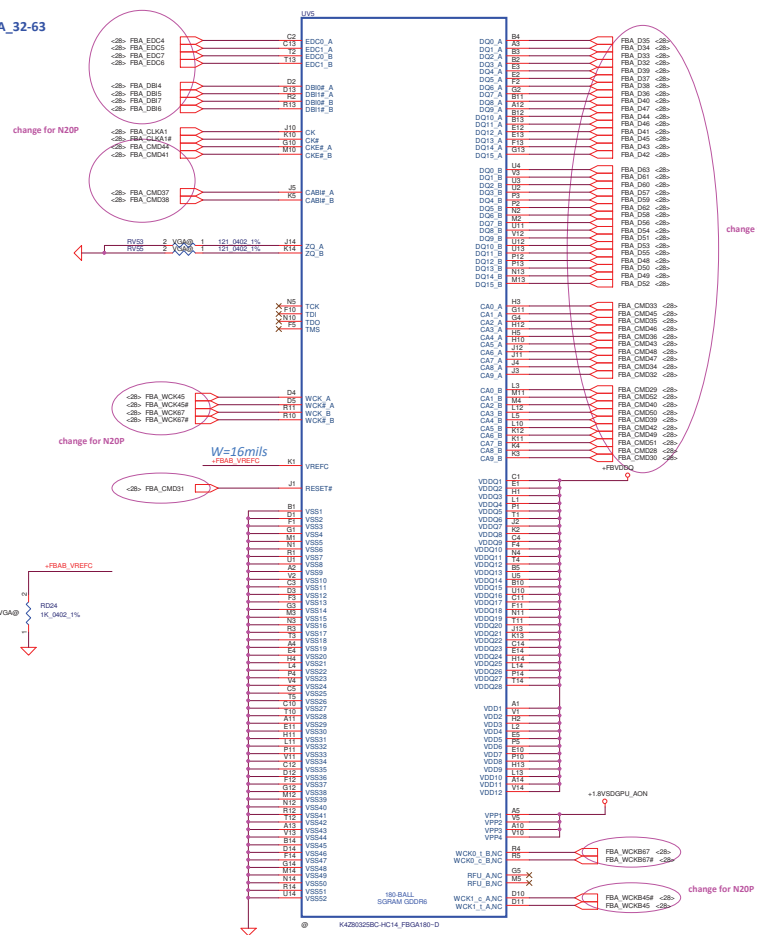




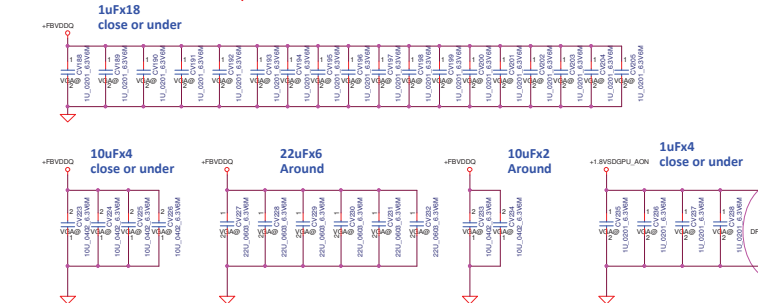
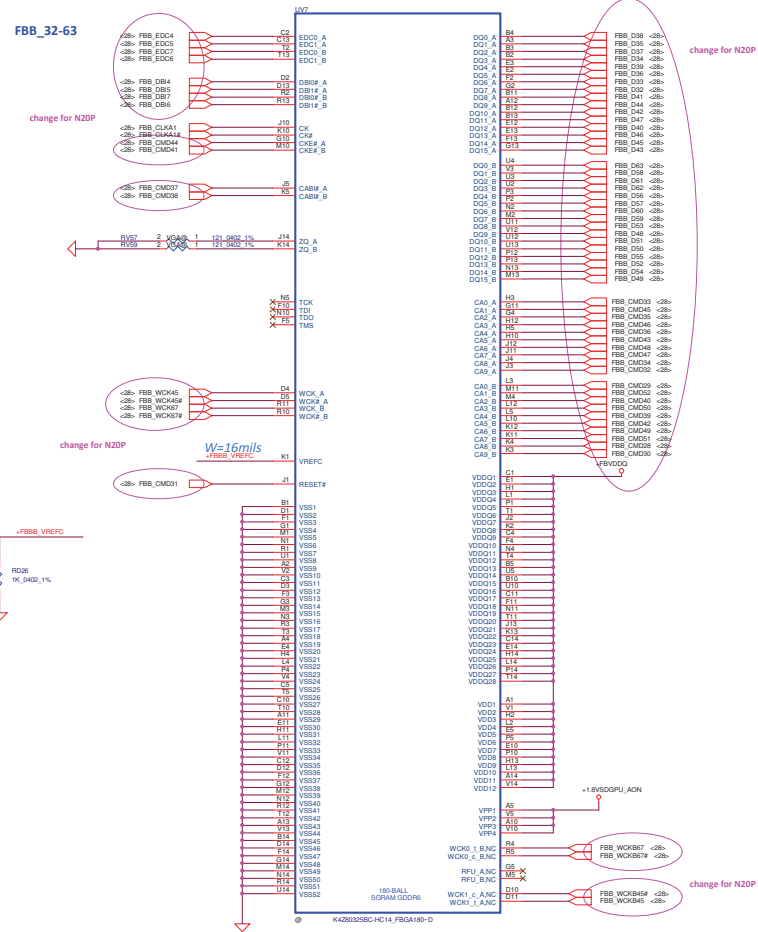
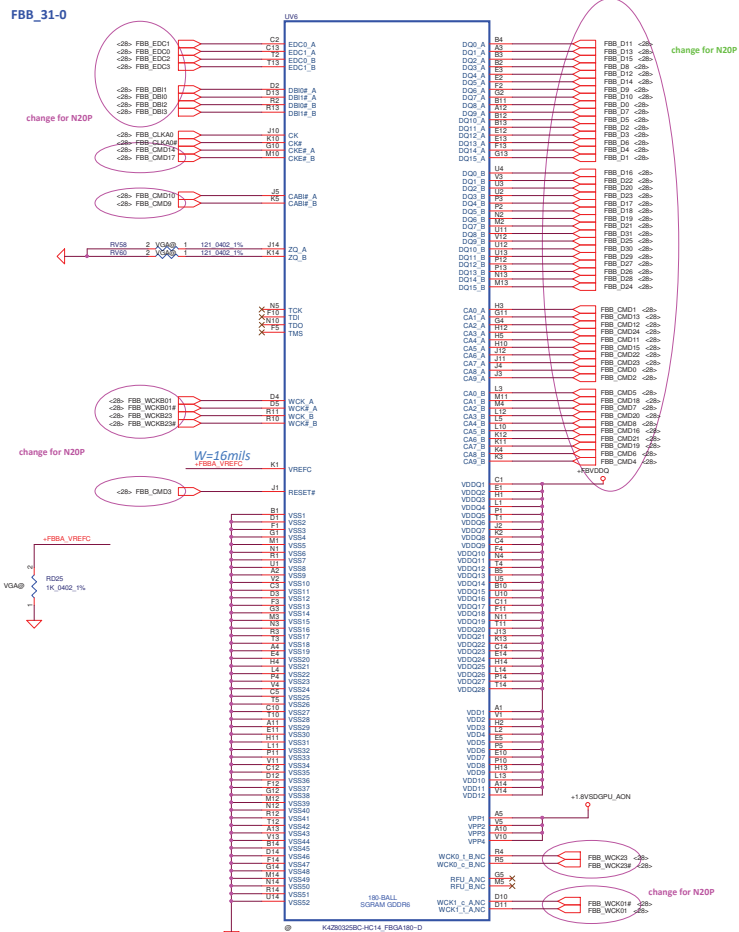
## FBA\_31-0



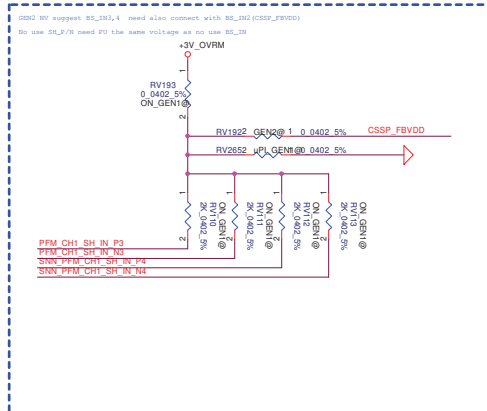
## FBA\_32-63



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		Date: 2021.09.28 10:51 Sheet 54 of 151



For OVRM Keep ON



UPI-Semi suggest pop CV274/CV271 when GEN2  
Keep NV suggest to unpop when GEN2.

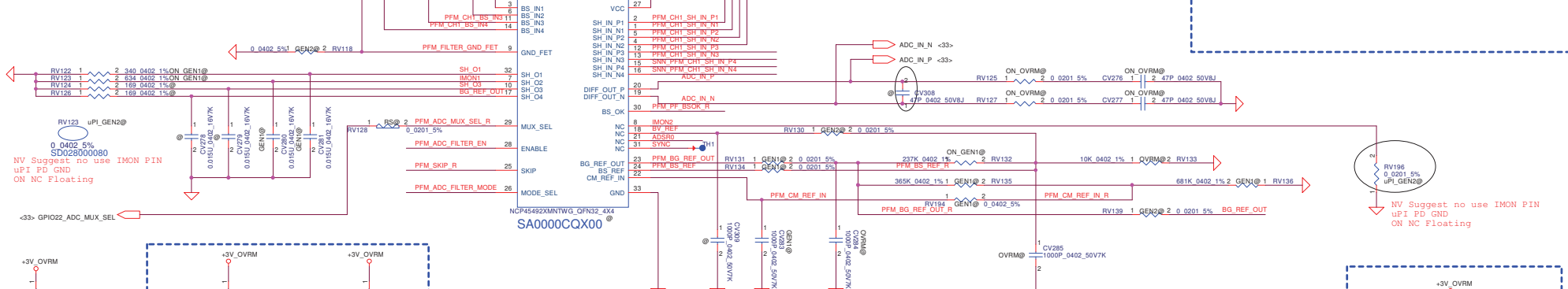


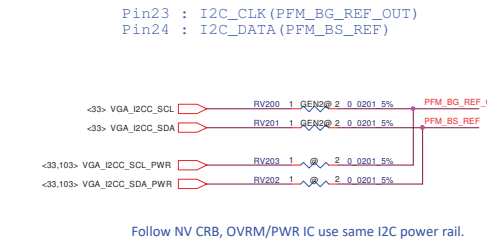
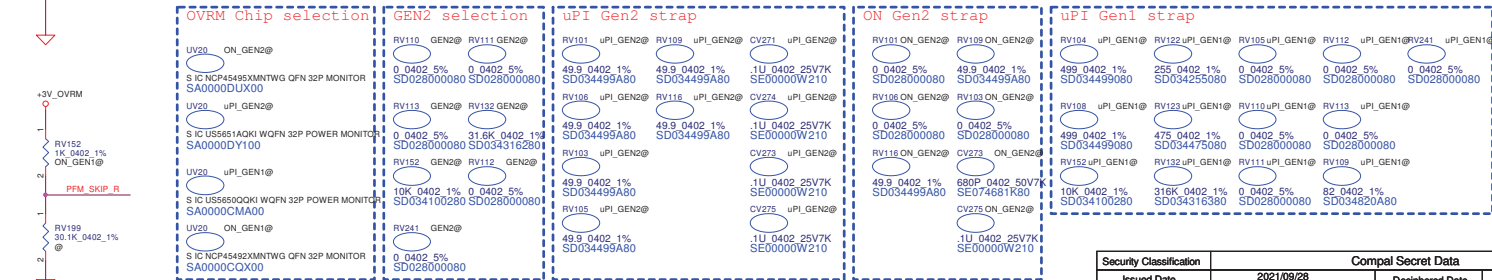
Table 3.6 OVR-M GEN1 BOM options based on GPU TGP

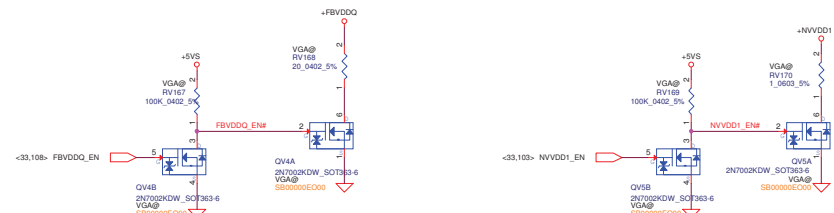
GPU Maximum TGP [W1]	Rsense [mohm]	UPI								OnSemi											
		SH_IN		SH_O		BUS PU		BUS PD		Bg_ref_o	SH_IN		SH_O		BUS PU		BUS PD		Bg_ref_o		
		RV103	RV241 RV109	RV122	RV123	RV106	RV108	RV104	RV108		RV103	RV241 RV109	RV122	RV123	RV106	RV108	RV104	RV108			
		R1	R3, R4	R21	R25	R22, R27	R23, R26	R17	R1	R3, R4	R21	R25	R22, R27	R23, R26	R17						
79 or lower [GB3B-64, GB3-64]	5	100Q	49.9Q	332Q	475Q	75KQ	499Q	316KQ	100Q	49.9Q	332Q	475Q	75KQ	499Q	316KQ	100Q	49.9Q	332Q	475Q	75KQ	499Q
79 or lower	5	100Q	49.9Q	357Q	357Q	75KQ	487Q	324KQ	100Q	49.9Q	357Q	357Q	75KQ	487Q	324KQ	100Q	49.9Q	357Q	357Q	75KQ	487Q
80-99	5	100Q	49.9Q	255Q	475Q	75KQ	499Q	316KQ	100Q	49.9Q	340Q	634Q	95KQ	665Q	243KQ	100Q	49.9Q	340Q	634Q	95KQ	665Q
100-170+	5	100Q	49.9Q	194Q	475Q	75KQ	499Q	316KQ	100Q	49.9Q	261Q	634Q	75KQ	665Q	237KQ	100Q	49.9Q	261Q	634Q	75KQ	665Q

**Note:** 1. GPU Maximum TGP [W] = Baseline TGP [W] + Configurable TGP Mode 2 [W] + Dynamic Boost 2.0 Maximum Power [W].  
Contact NVIDIA Application Engineering for VBIOS with OVR-M Gen 1 BOM configuration.

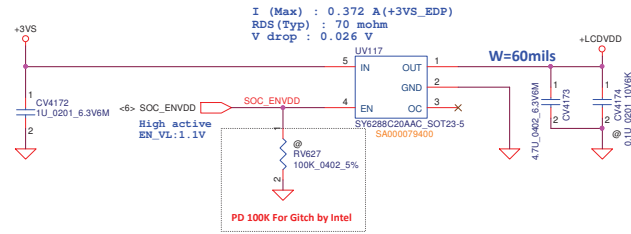
BOM option

ON_GEN1	OVRM@/GEN1@/ON_OVRM@/ON_GEN1@
ON_GEN2	OVRM@/GEN2@/ON_OVRM@/ON_GEN2@
uPI_GEN1	OVRM@/GEN1@/uPI_GEN1@
uPI_GEN2	OVRM@/GEN2@/uPI_GEN2@

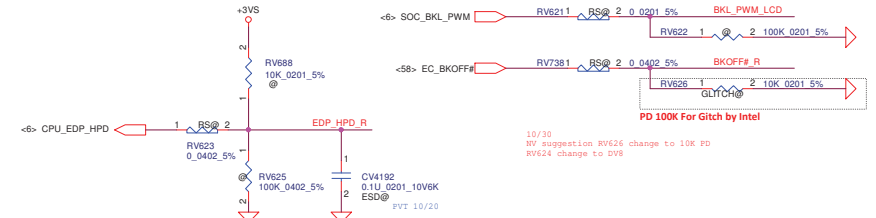




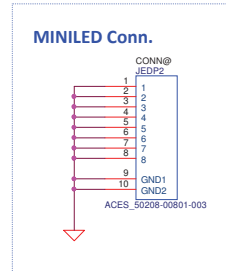
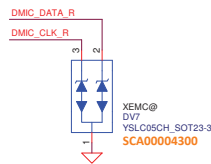
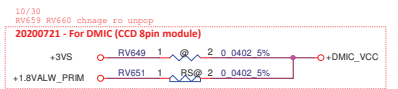
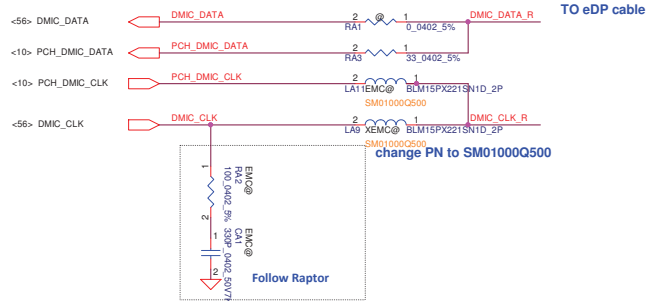
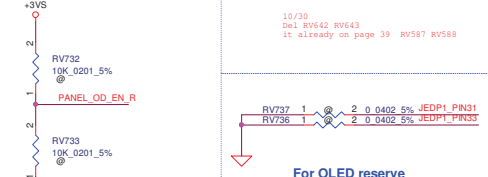
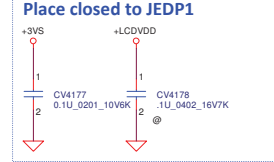
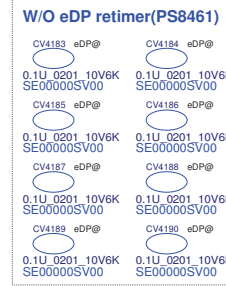
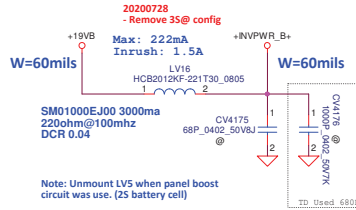
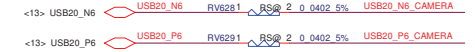
# LCD POWER CIRCUIT



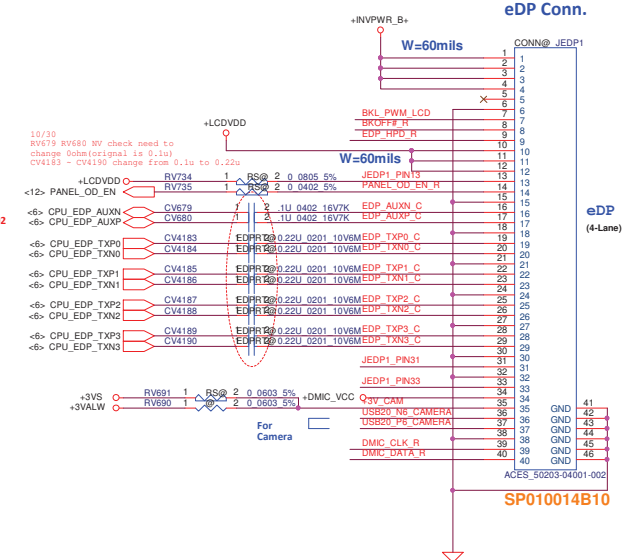
# LCD enable signal



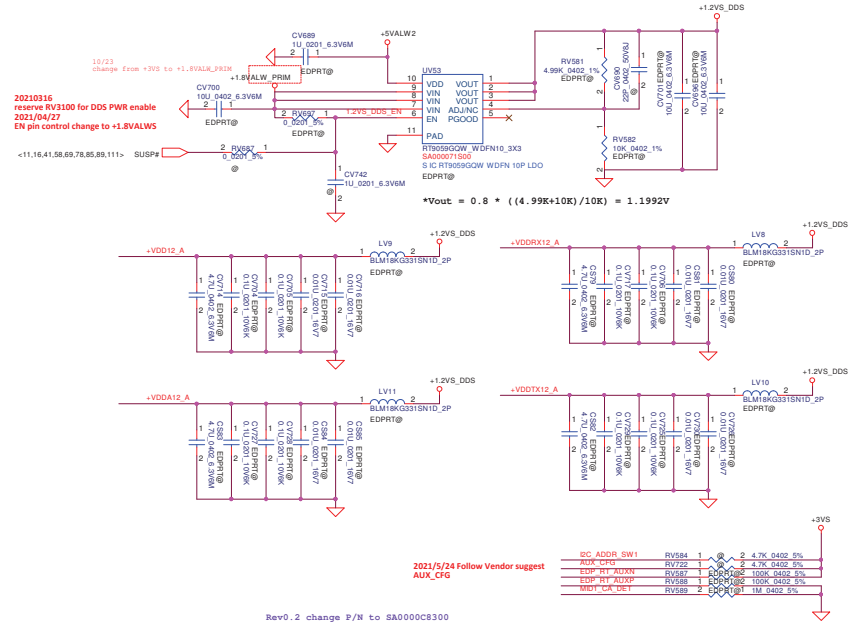
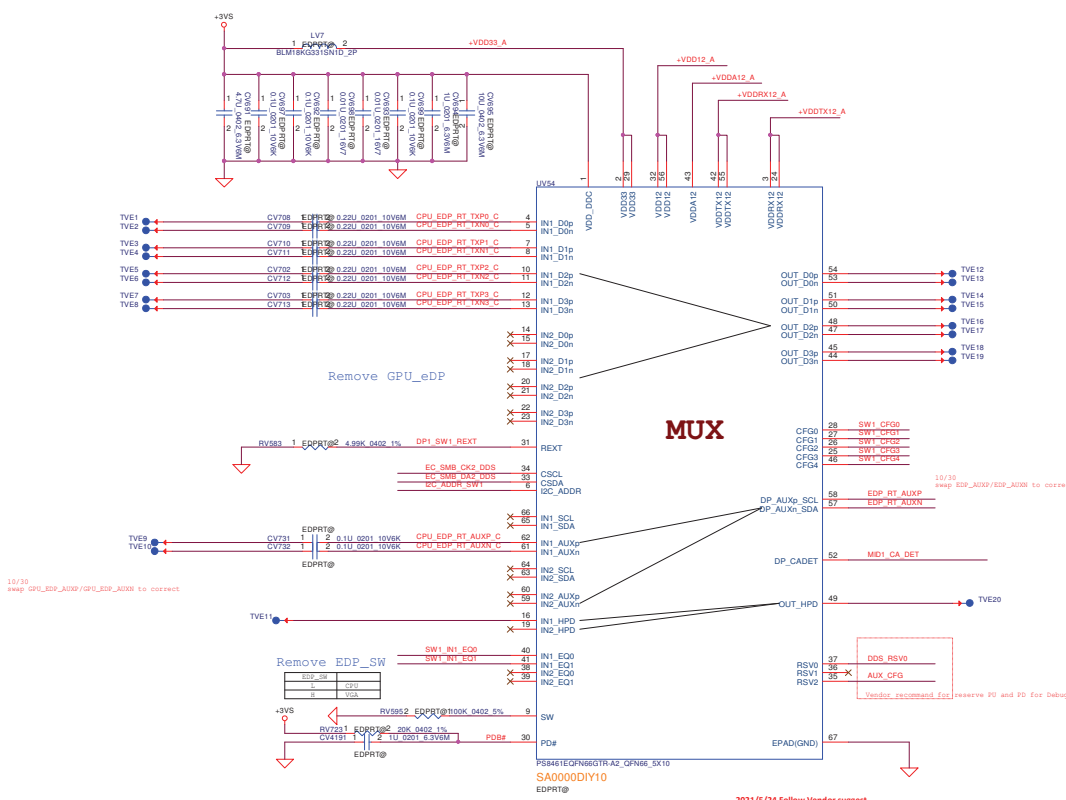
# Camera



**2021/4/27 RV679 and RV680**  
**change from 0ohm to 0.1u 0.0402**



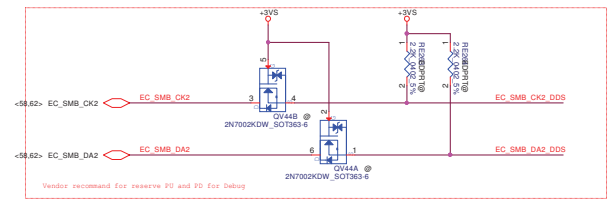
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								Size		Document Number		Rev	
								LA-L973P		1.0			
								Date:		Thursday, October 26, 2021			
								I Sheet		38 of 121			



Remove BL Switch

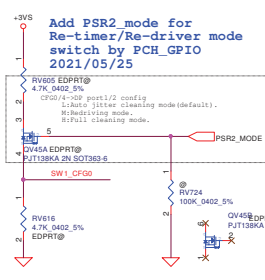
Remove ENVDD Switch

Remove PWM Switch



Pin	Signal	Value
1	SW1_INI_E0P	4.7K 0402 5%
2	SW1_INI_E0N	4.7K 0402 5%
3	SW1_INI_E0P	4.7K 0402 5%
4	SW1_INI_E0N	4.7K 0402 5%
5	SW1_INI_E0P	4.7K 0402 5%
6	SW1_INI_E0N	4.7K 0402 5%
7	SW1_INI_E0P	4.7K 0402 5%
8	SW1_INI_E0N	4.7K 0402 5%
9	SW1_INI_E0P	4.7K 0402 5%
10	SW1_INI_E0N	4.7K 0402 5%
11	SW1_INI_E0P	4.7K 0402 5%
12	SW1_INI_E0N	4.7K 0402 5%
13	SW1_INI_E0P	4.7K 0402 5%
14	SW1_INI_E0N	4.7K 0402 5%
15	SW1_INI_E0P	4.7K 0402 5%
16	SW1_INI_E0N	4.7K 0402 5%
17	SW1_INI_E0P	4.7K 0402 5%
18	SW1_INI_E0N	4.7K 0402 5%
19	SW1_INI_E0P	4.7K 0402 5%
20	SW1_INI_E0N	4.7K 0402 5%

CFG0/4-VOP port1/2 config  
 i-Auto jitter cleaning mode(default).  
 W-Reducing mode.  
 H-Full cleaning mode.  
 CFG1/3-Auto EQ option for port1/2  
 i-Auto EQ enable, EQ auto adjust base on link training(default).  
 H-Auto EQ disable.  
 CFG2-VOP output config  
 i-Dynamic adjust base on link training(default).  
 H-Fix on 400mV/50mV  
 H-Fix on 100mV/1.5mV

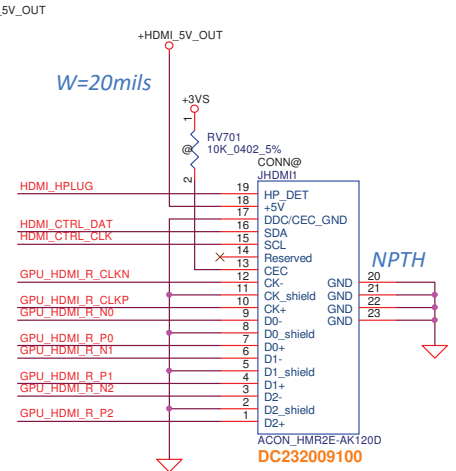
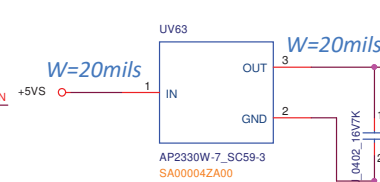
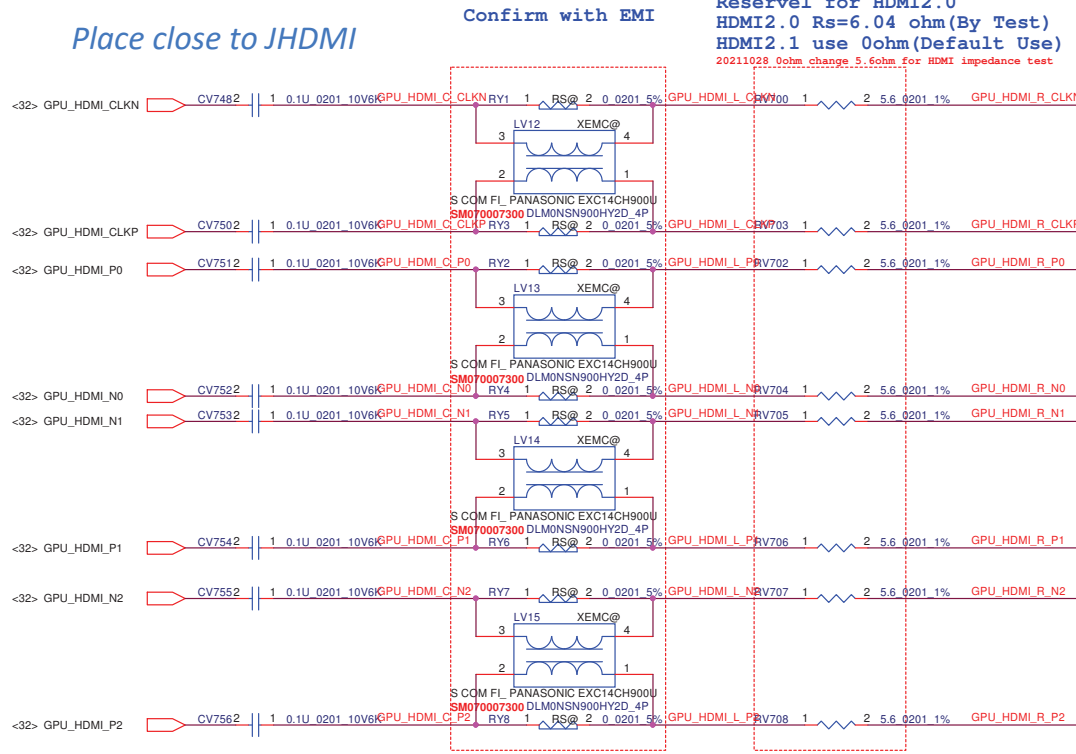




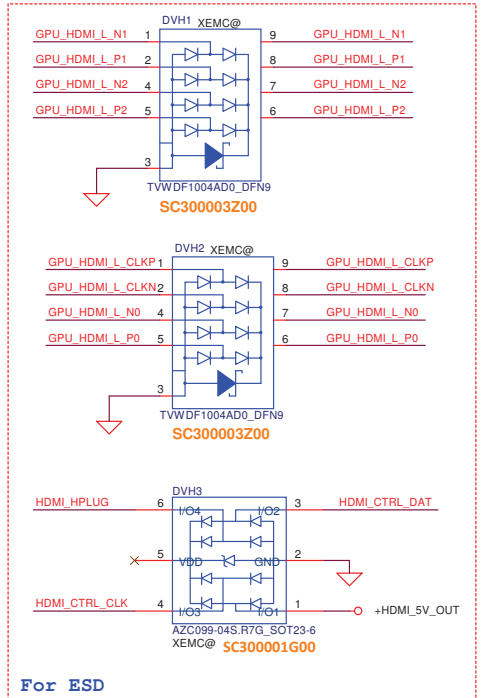
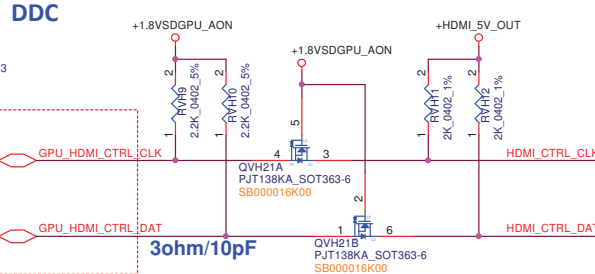
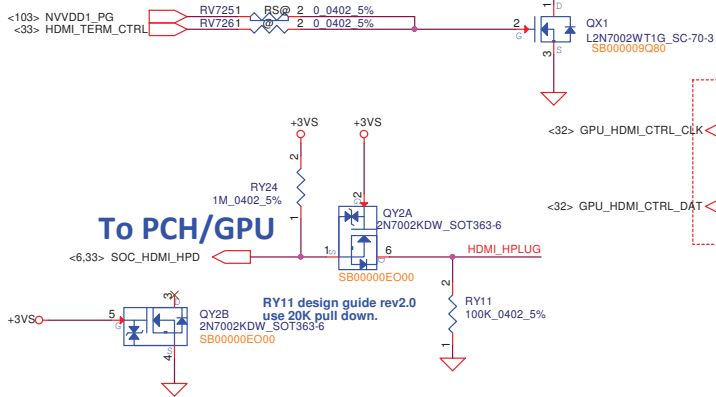
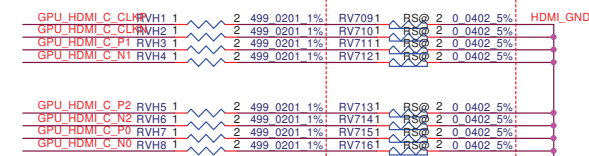
Place close to JHDMI

Confirm with EMI

Reservel for HDMI2.0  
HDMI2.0 Rs=6.04 ohm(By Test)  
HDMI2.1 use 0ohm(Default Use)  
20211028 0ohm change 5.6ohm for HDMI impedance test

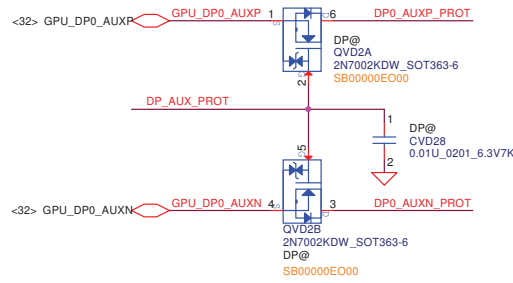
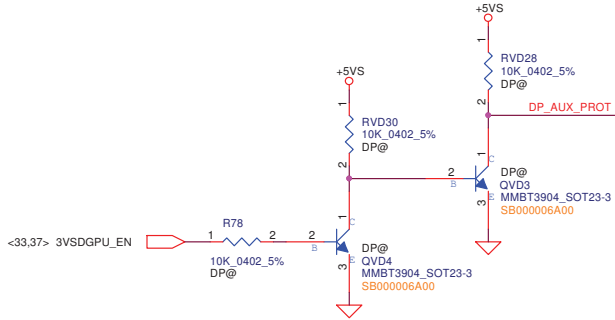


Reservel for HDMI2.0 bead SM01000LP00

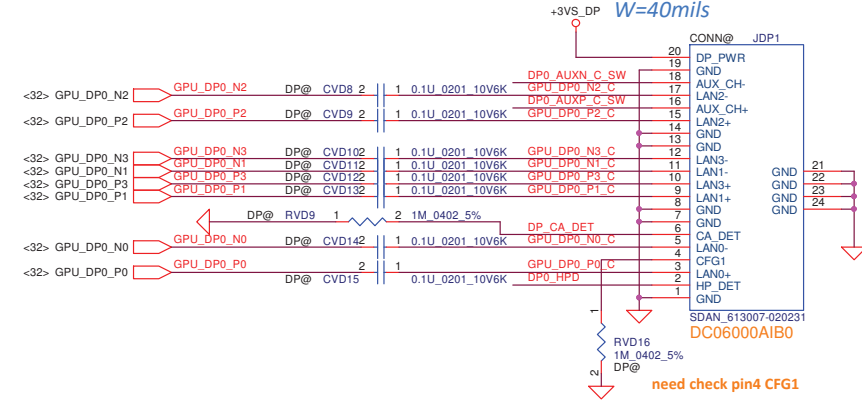
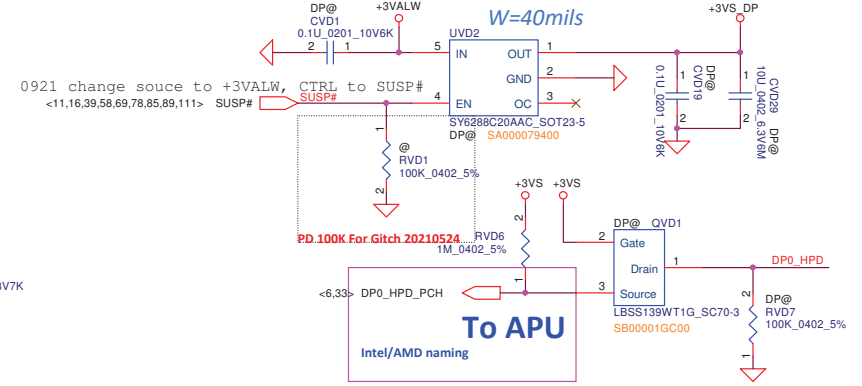
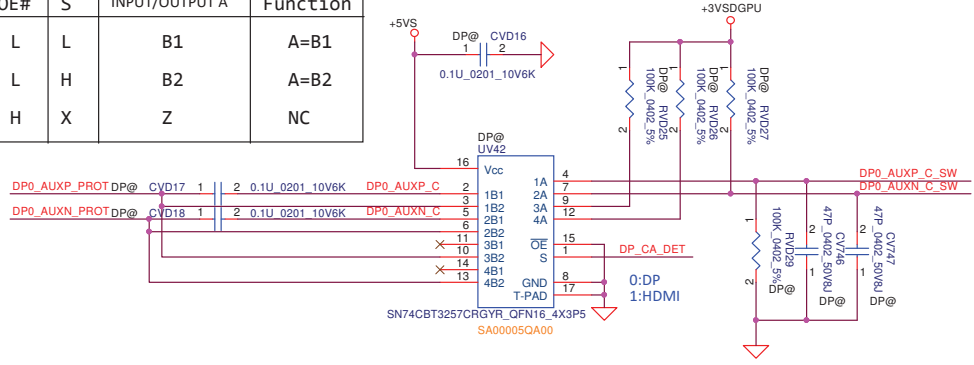


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Date:				Monday, November 08, 2021	Sheet	40 of 121

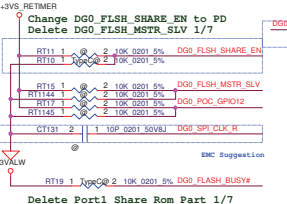




OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC



### MB\_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)



```

DG1_RST#:  

For PD based systems, DG1_RST# should be output from PD.  

For TPC based systems, DG1_RST# should be output from SOC/EC.  

DG1_BB_FORCE_FWR:  

Connect to EC/PCB for FW update  

'0' - by default  

'1' - for debug only

```

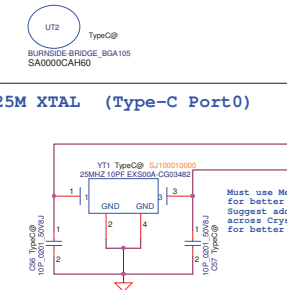
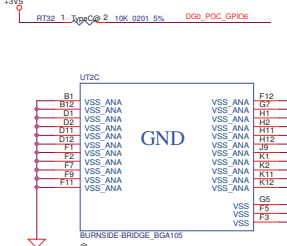
```

If Flash sharing is being used, PD should be used.
If Flash sharing isn't being used, PD should be used.

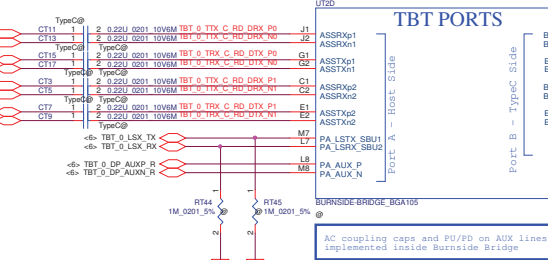
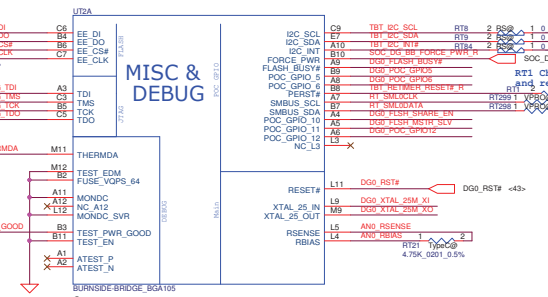
DGL_FLASH_SHARE_EN:
'0' - Flash isn't shared. 1 Flash per Re-timer
'1' - Flash is shared between 2 Re-timers

DGL_FLASH_MSTR_SLV:
'0' - Set Re-timer to be Slave on shared flash SPI I/F.

```



## TAG (Type-C Port0)

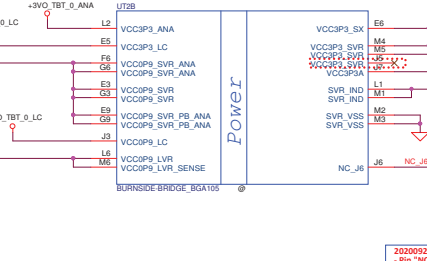


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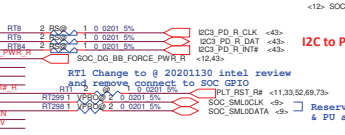
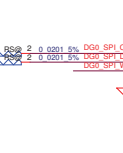
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S



## type-C Port0)

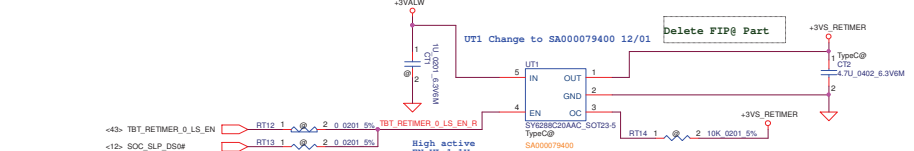


DG0 RST# <43>

- Follow E team design PD 100K
- SMBUS:
  - No support Vpro
  - Intel recommended PD 100K

## SPORTS

---



**I2C to PD, SOC**

- +3VS\_RETIMER\_0 Tolerance (at 5%/-7.5%):
- Burnside Bridge power pins which connected to +3VS\_RETIMER\_0 should be 3.465v maximum and 3.07v minimum for normal operation.
- +3VS\_RETIMER\_0 ripple: 40mVp-p

**I2S (Max) : 0.37 A (+3V\_PRIM)**

**RS (Typ) : 70 mohm**

**V drop : 0.026 V**

PLT\_RST\_R# <11.33,52.69,73>  
SOC\_SML0CLK <-> Reserved v-pro only  
SOC\_SML0DATA <-> PU at CPU side

RT42 pop PH change to +3VS\_Retimer 20201130 Intel review +3VS\_RETIMER

TBT\_RETIMER\_RESETE\_R RT42 2 1 10K 0201 5%  
RT43 2 1 10K 0201 5%

RTH4 2 1 1026 50% GC  
 RTH5 2 1 1026 50% GC

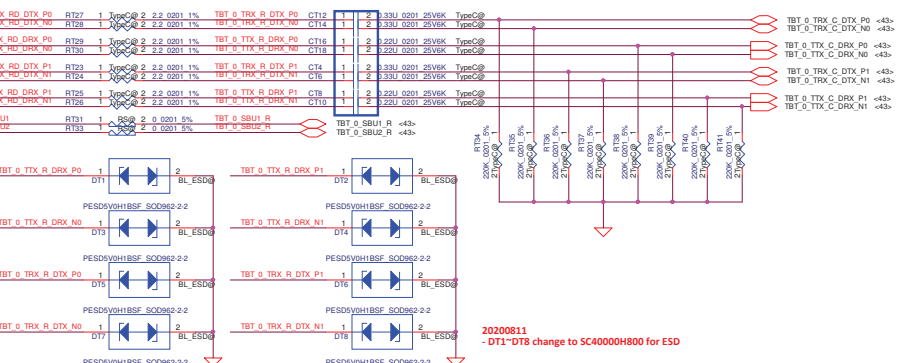
W E team design PD 100K

JS:

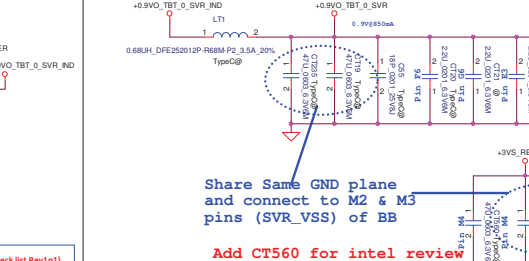
upport Vpro

recommended PD 100K

NOTE:  
Re-Timer with TBT , AC Caps should be use 0201/25V package.  
Re-Timer without TBT , AC Caps can be use 0402/25V package.  
For non-PD support 25V rating is no must.

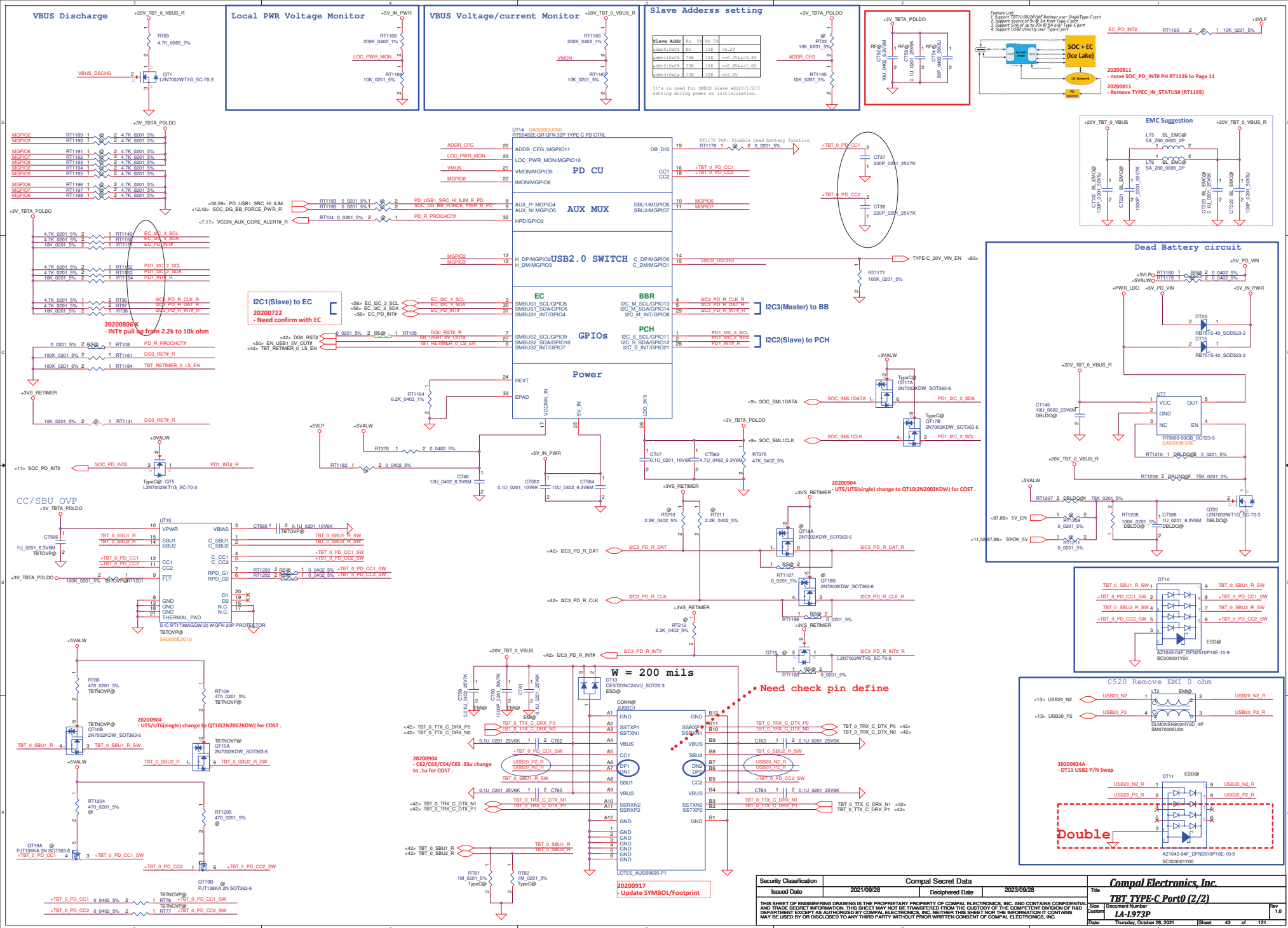


## Power Supply Decoupling of Type-C Port0



All 0201 decoupling caps should be placed as close as possible to the re-timer power pins

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# Reserve Page

# Reserve Page

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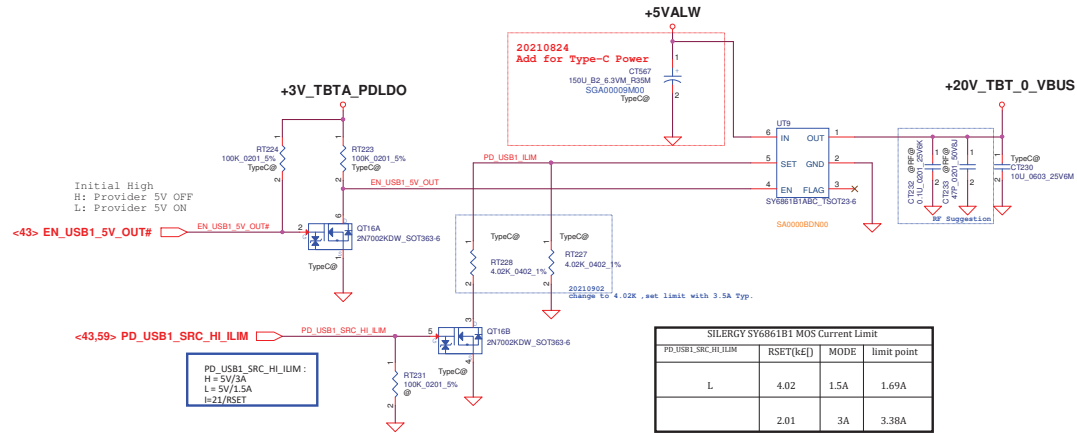
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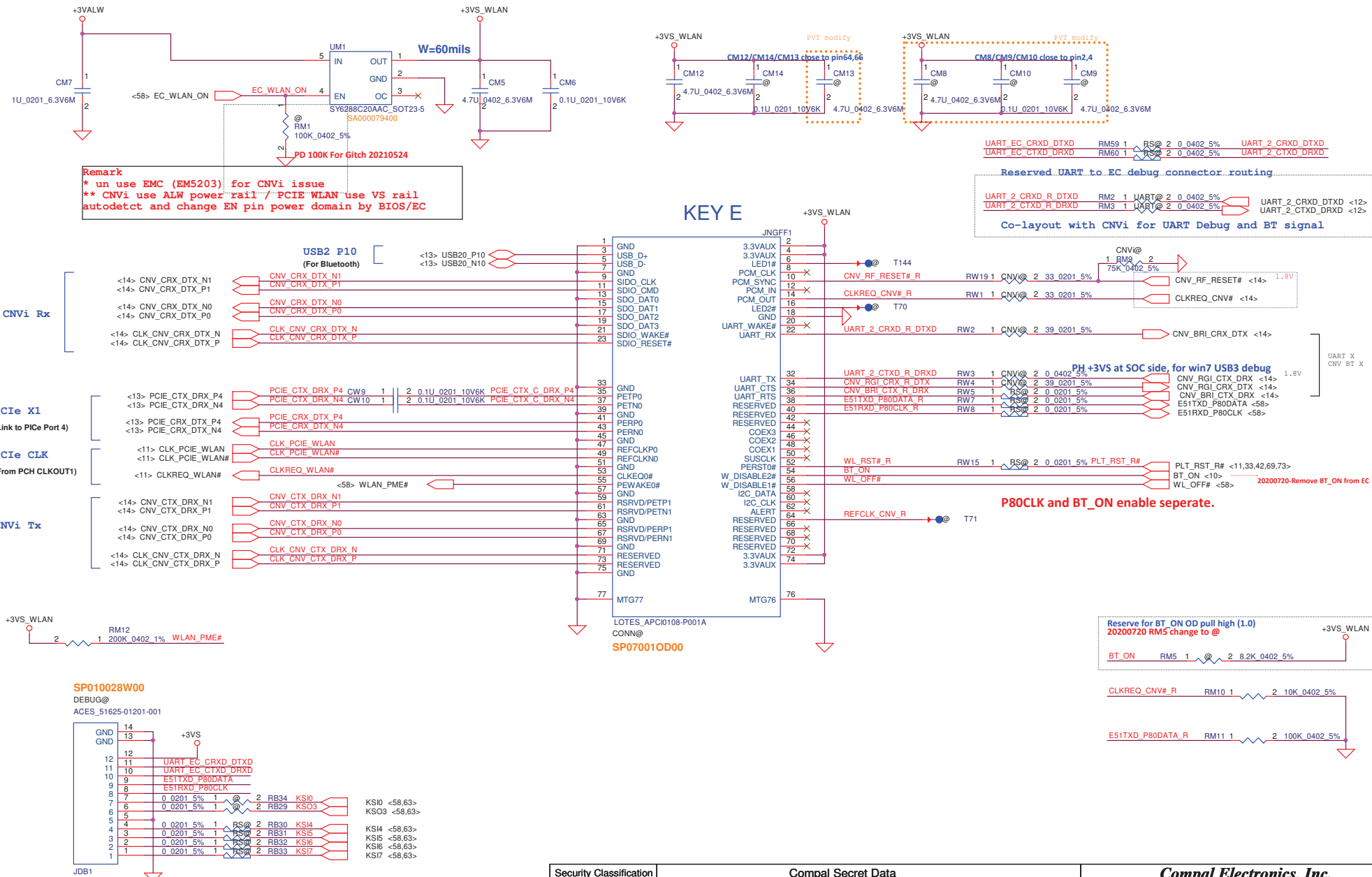
MB\_USB3.1 TypeC Conn. (Power Path)  
- For Realtek 5452E



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## NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



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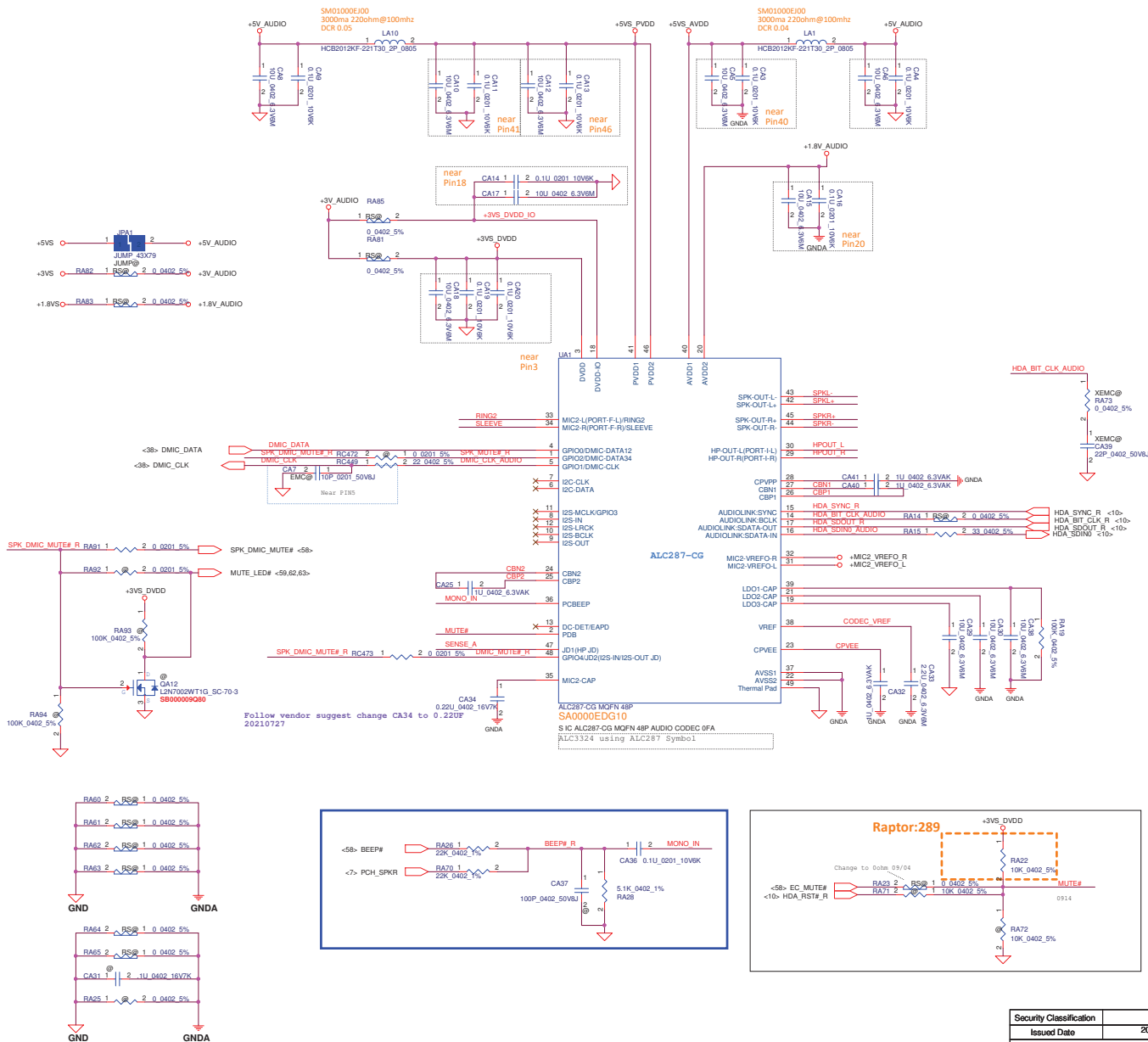
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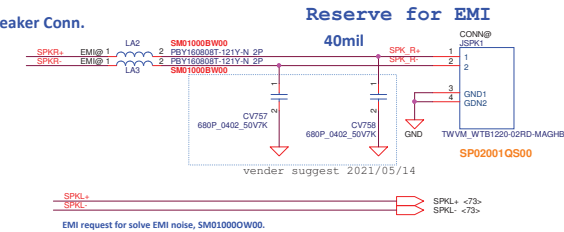
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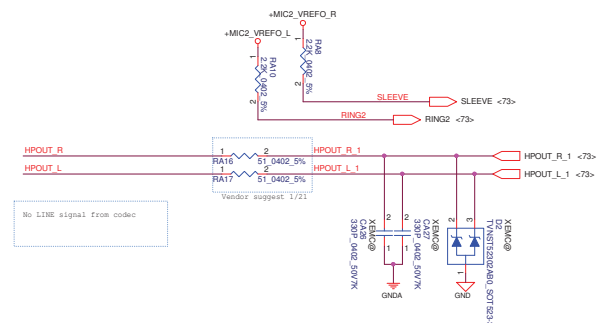
# HD Audio Codec



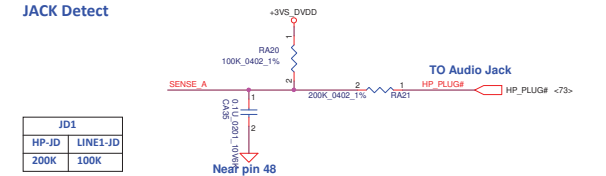
## Int. Speaker Conn.



## Headphone Out



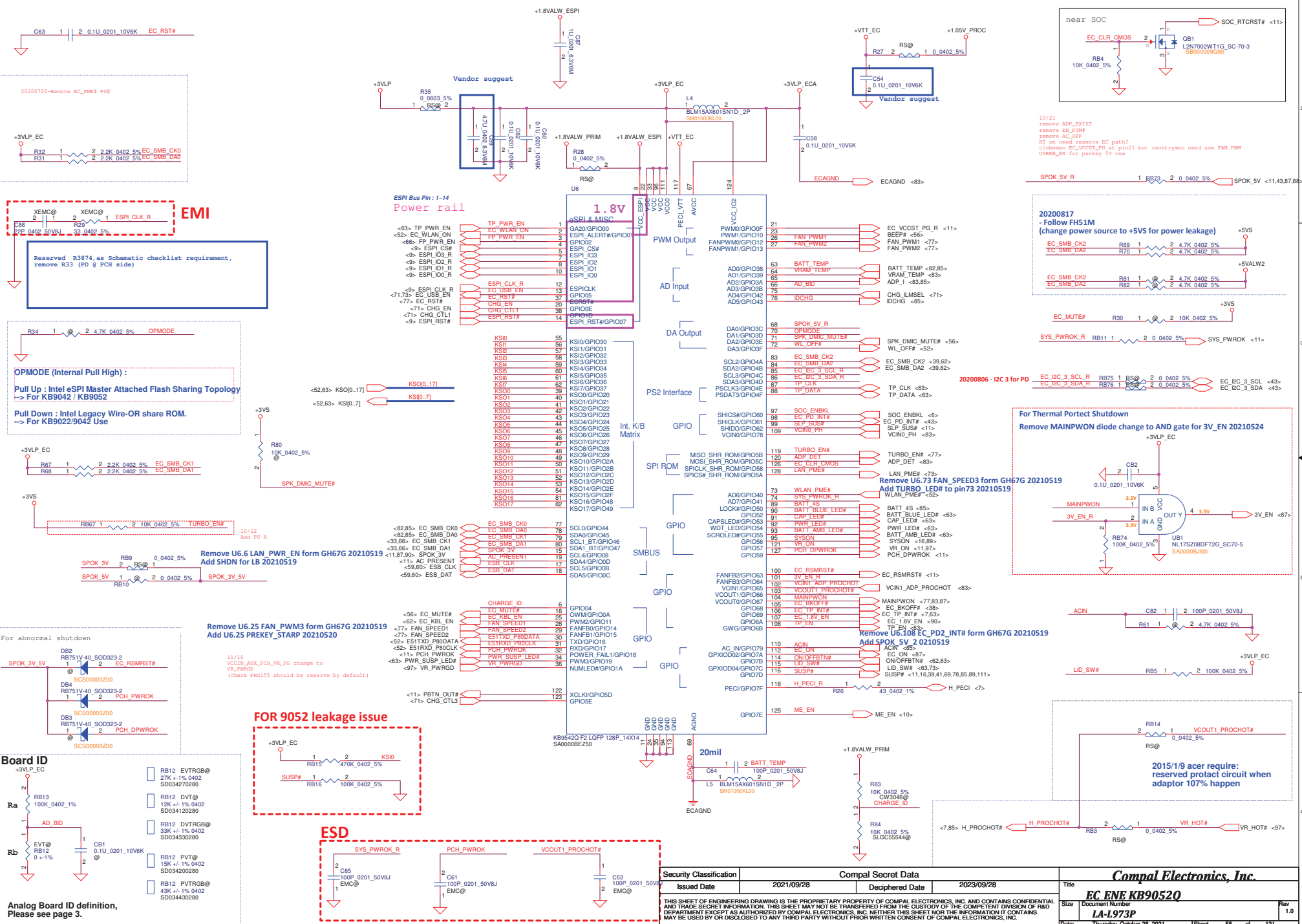
## JACK Detect





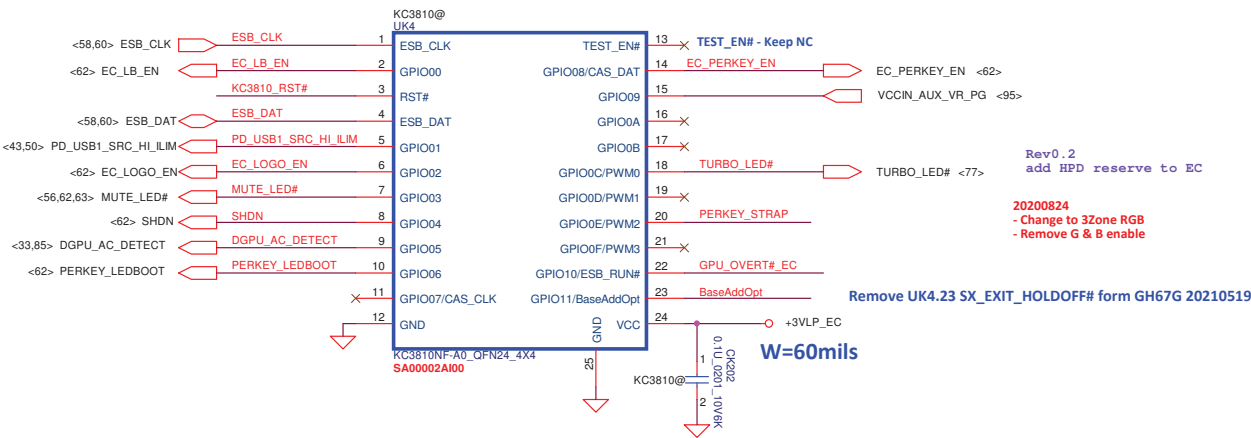
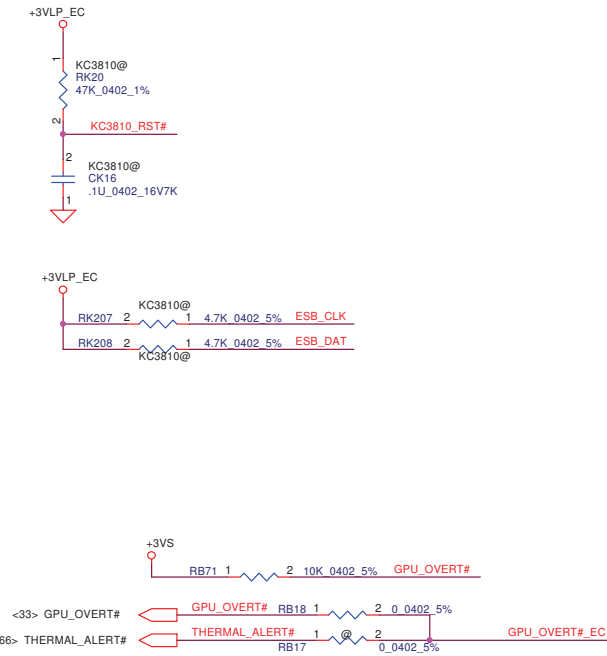
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				Date:	Thursday, October 28, 2021
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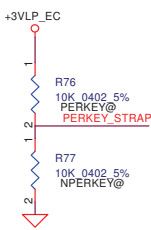


OMEN New ESB CLK&DAT for Extend I/O

\*NMI\_DBG#: is a debug pin for EC to  
infrom BIOS after press hot key.



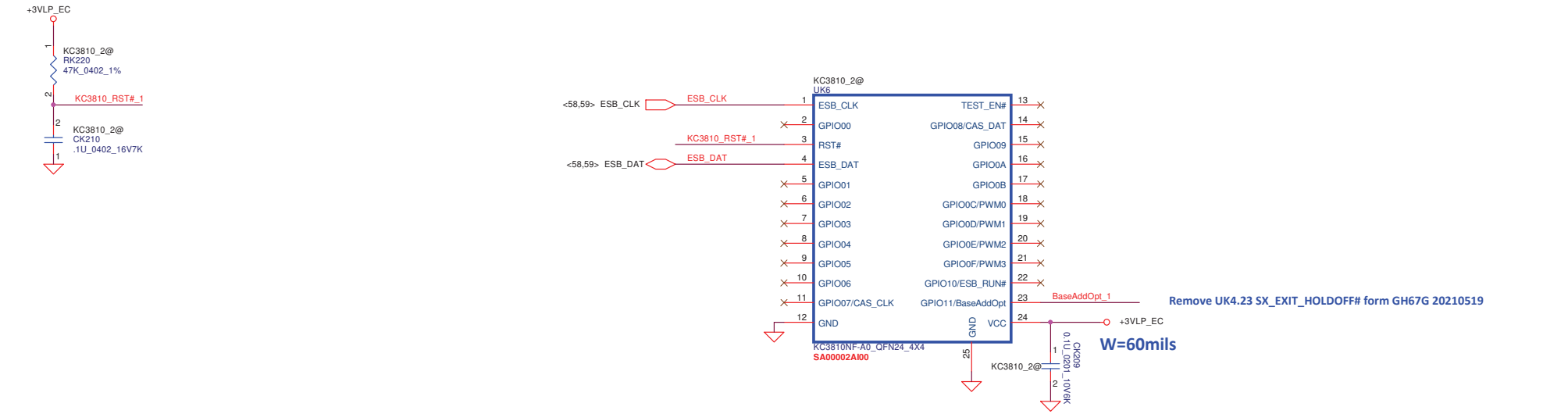
Need EC confirm



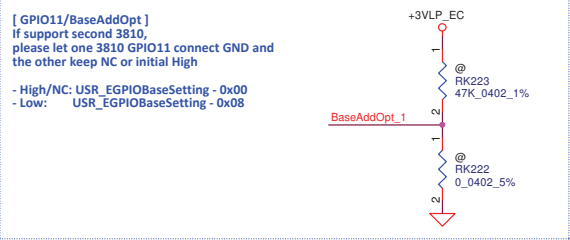
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1.0		LA-L973P		Rev	

OMEN New ESB CLK&DAT for Extend I/O

\*NMI\_DBG#: is a debug pin for EC to  
infrom BIOS after press hot key.



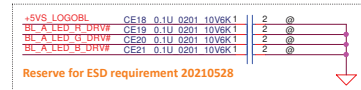
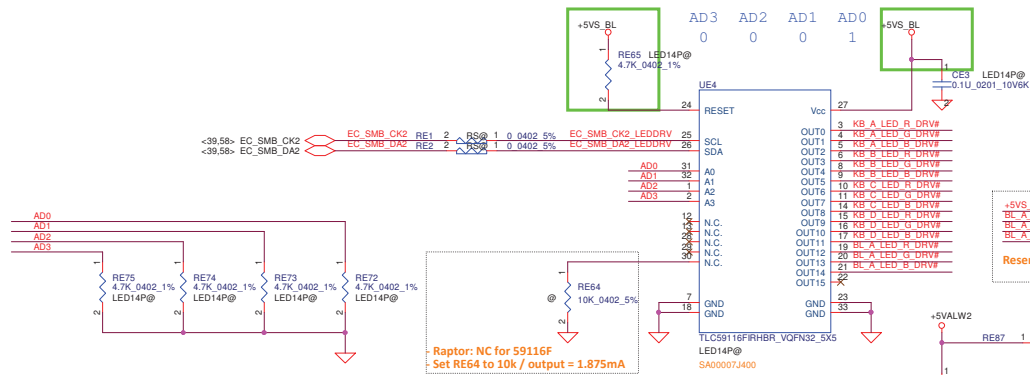
Need EC confirm



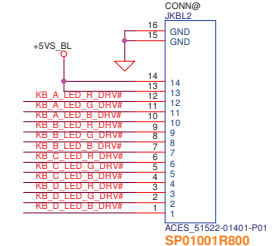
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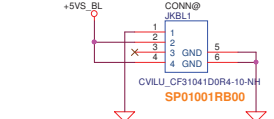
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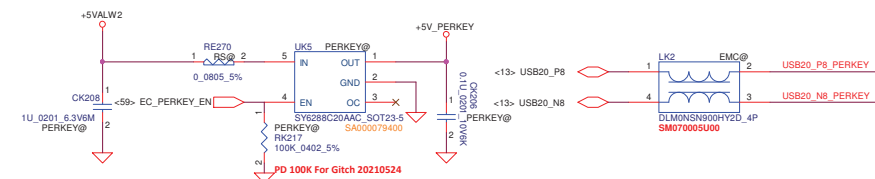
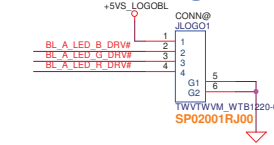
## RGB KB Backlight Conn



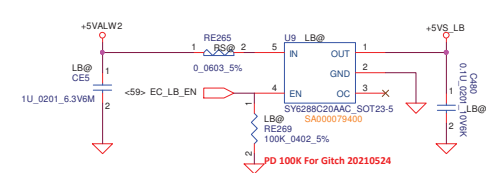
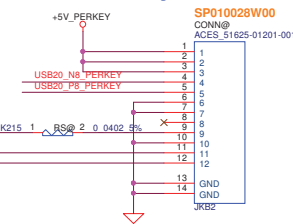
## Single BackLight Conn



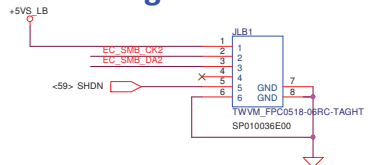
## LOGO BackLight Conn



## Per Key Conn.



## LightBar Conn



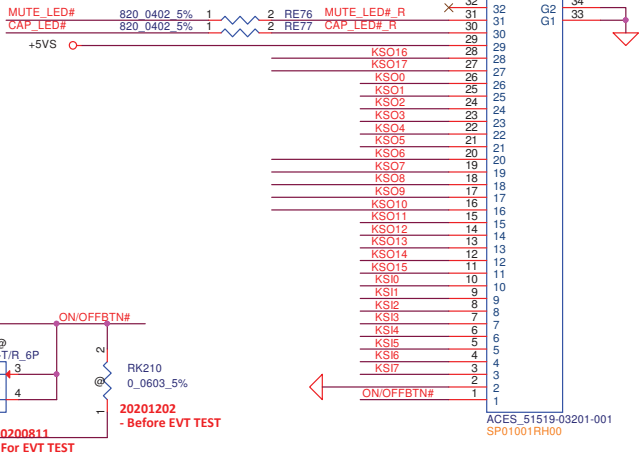
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# KB Conn. 32pin

DVT: remove SWK1 switch button

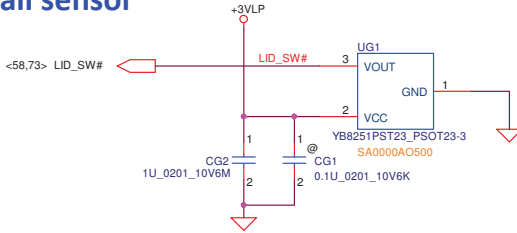
## ON/OFF BTN

<56,59,62> MUTE\_LED#  
<58> CAP\_LED#

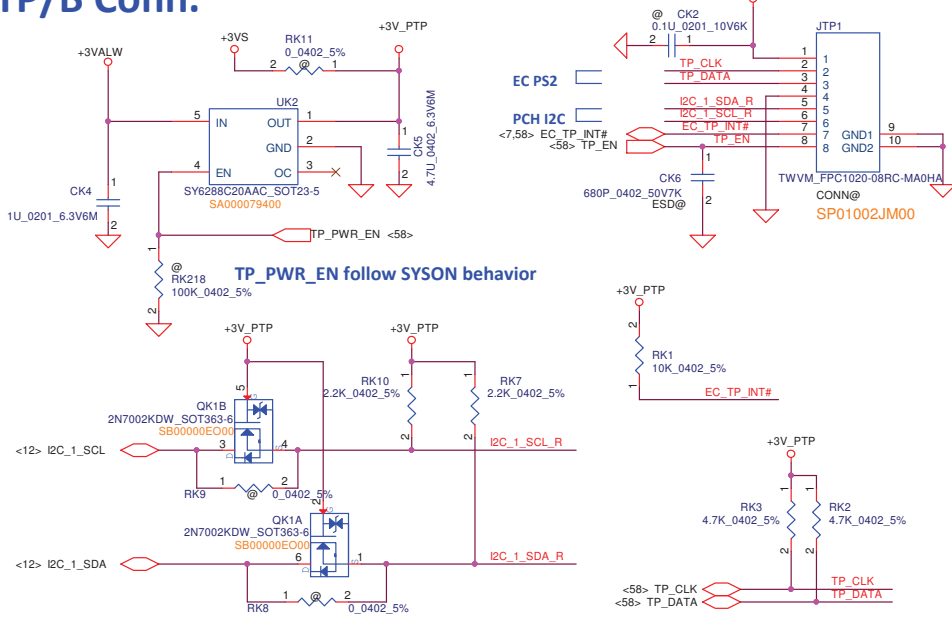


ON/OFFBTN#	CE22	1000P	0201	50V7K	1	2	XESD@
KSO6	CE6	1000P	0201	50V7K	1	2	ESD@
KSO7	CE7	1000P	0201	50V7K	1	2	ESD@
KSO8	CE8	1000P	0201	50V7K	1	2	ESD@
KSO9	CE9	1000P	0201	50V7K	1	2	ESD@
KSO10	CE10	1000P	0201	50V7K	1	2	ESD@
KSO16	CE11	1000P	0201	50V7K	1	2	ESD@
KSO17	CE12	1000P	0201	50V7K	1	2	ESD@

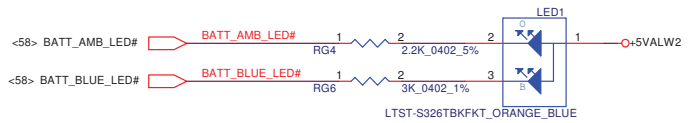
## Hall sensor



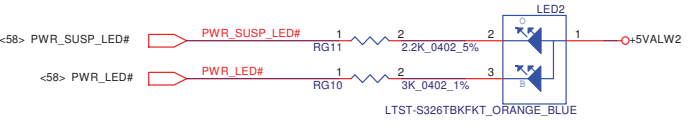
# TP/B Conn.



# Battery LED



## Power LED



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						Size		Document Number		Rev	
						Custom		LA-L973P		1.0	
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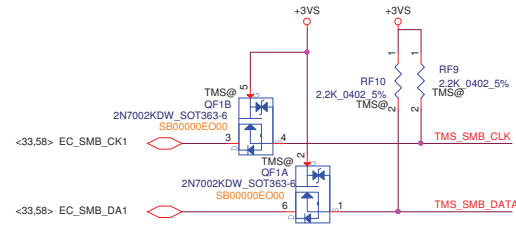
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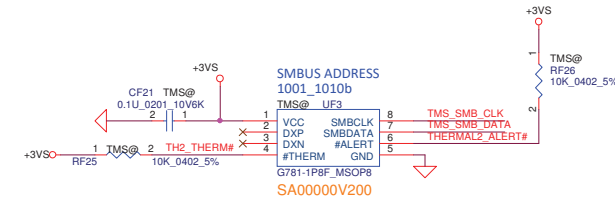
20200717  
- Remove G-Sensor

## THERMAL SENSOR

20200810  
- Check address

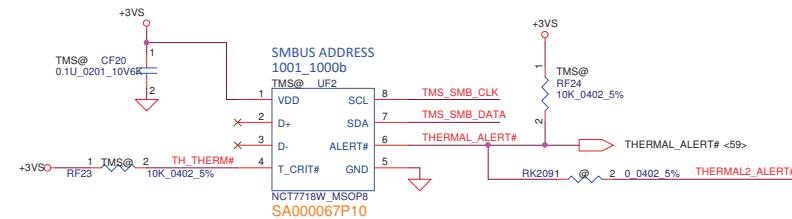


Close to Thermal SKIN



20200928  
- Remove 3rd thermal sensor

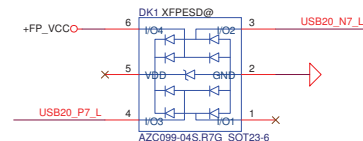
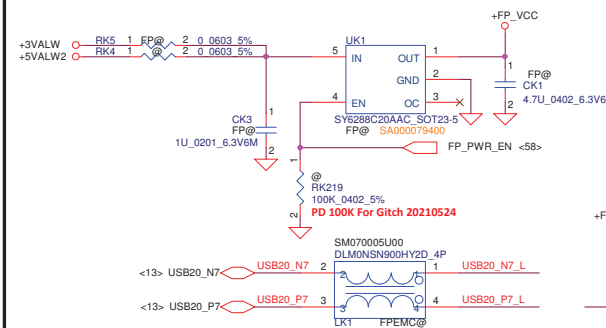
Close to SO-DIMM



## TPM 2.0

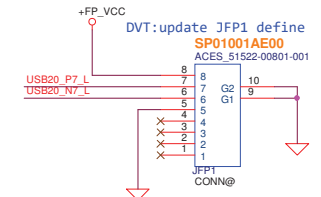
20210528 remove TPM

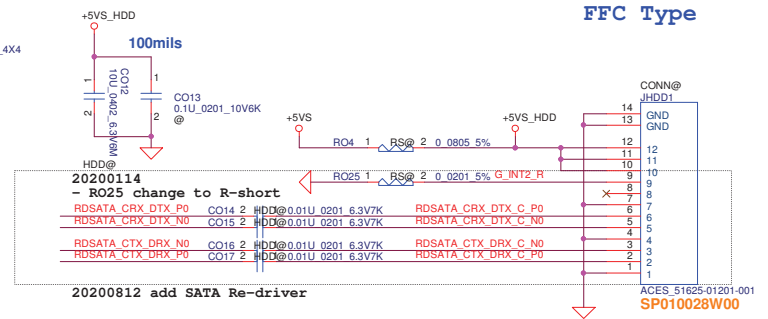
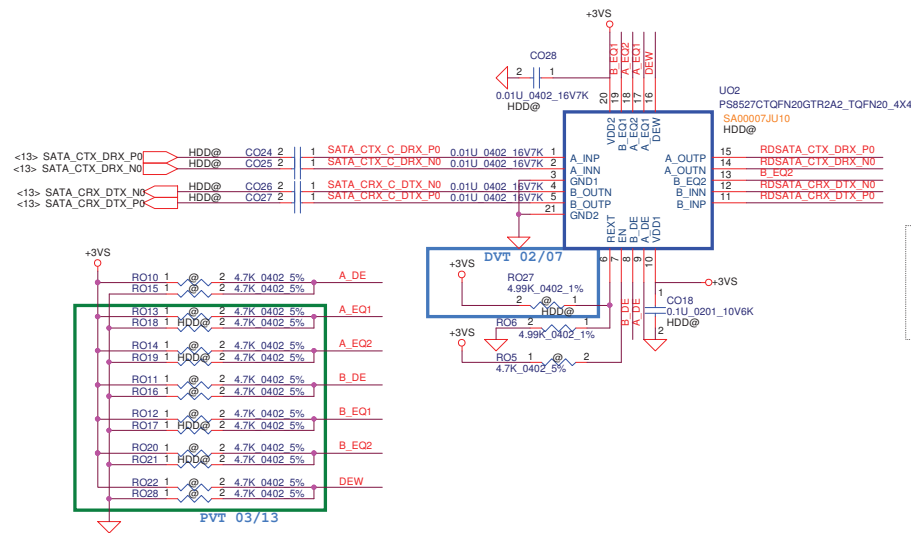
## Finger print



PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

Power Source Check  
EGIS ETU801 +FP\_VCC=5V  
ELAN SA464K-2200 +FP\_VCC=3.3V





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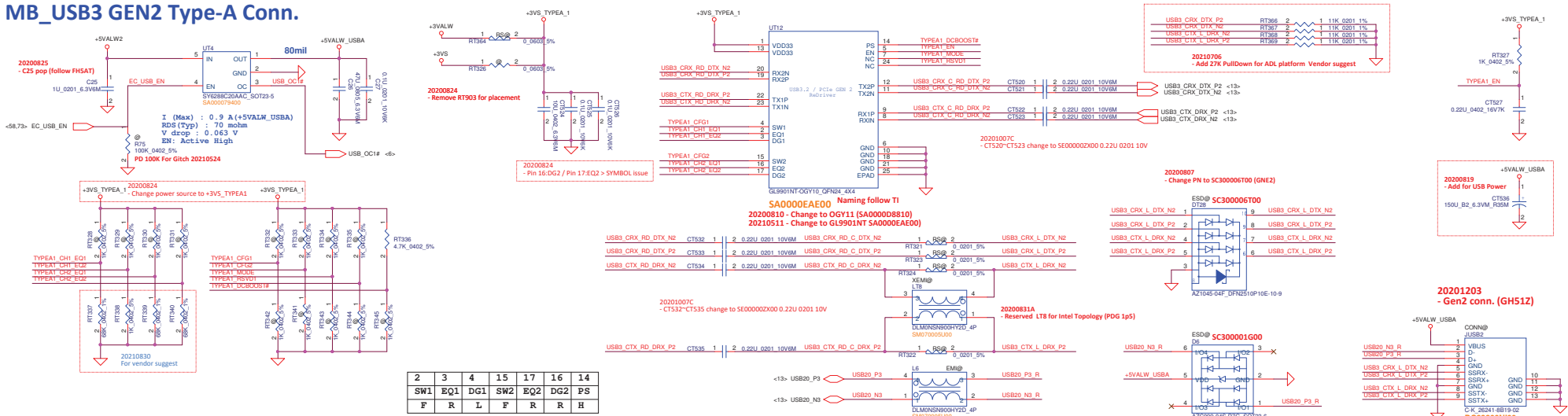


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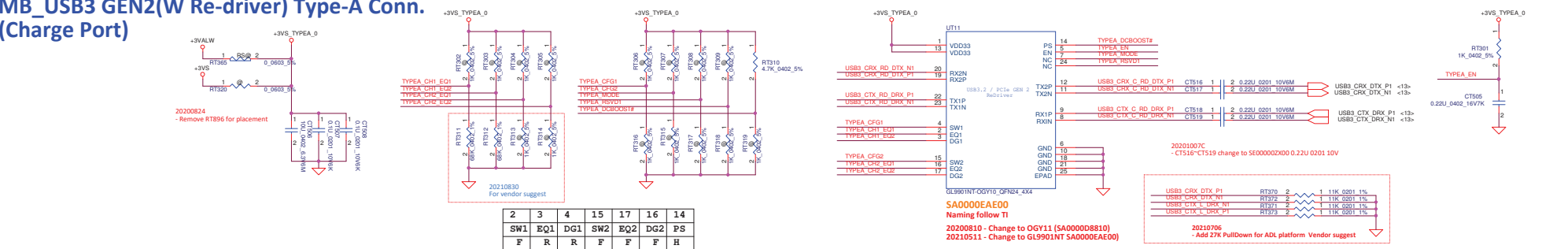
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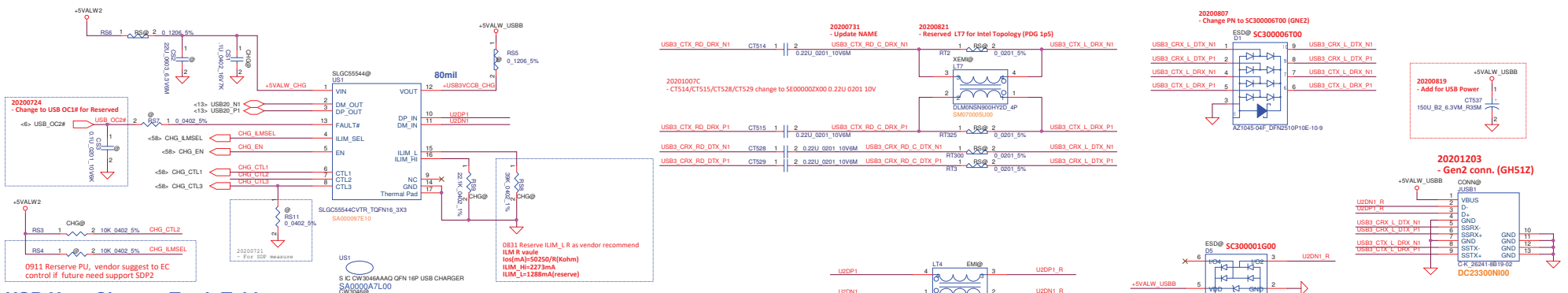
## MB\_USB3 GEN2 Type-A Conn.



### MB\_USB3 GEN2(W Re-driver) Type-A Conn. (Charge Port)



## USB Host Charger



## USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

ZZZ X76CWⓈ  
ALT. GROUP PARTS BC1.2 CW3046 HH514  
**X76869BOLCJ**

ZZZ X76SLGCⓈ  
ALT. GROUP PARTS BC1.2 SLG55544 HH514  
**X76869BOLCK**

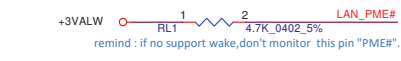
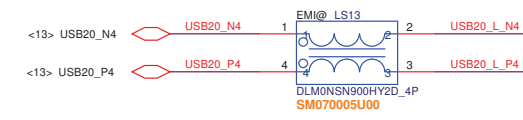
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Issued Date	2021/08/28	Deciphered Date	2023/08/28	<b>USB2/USB3 TYPEA1&amp;2</b> <b>LA-1973P</b>
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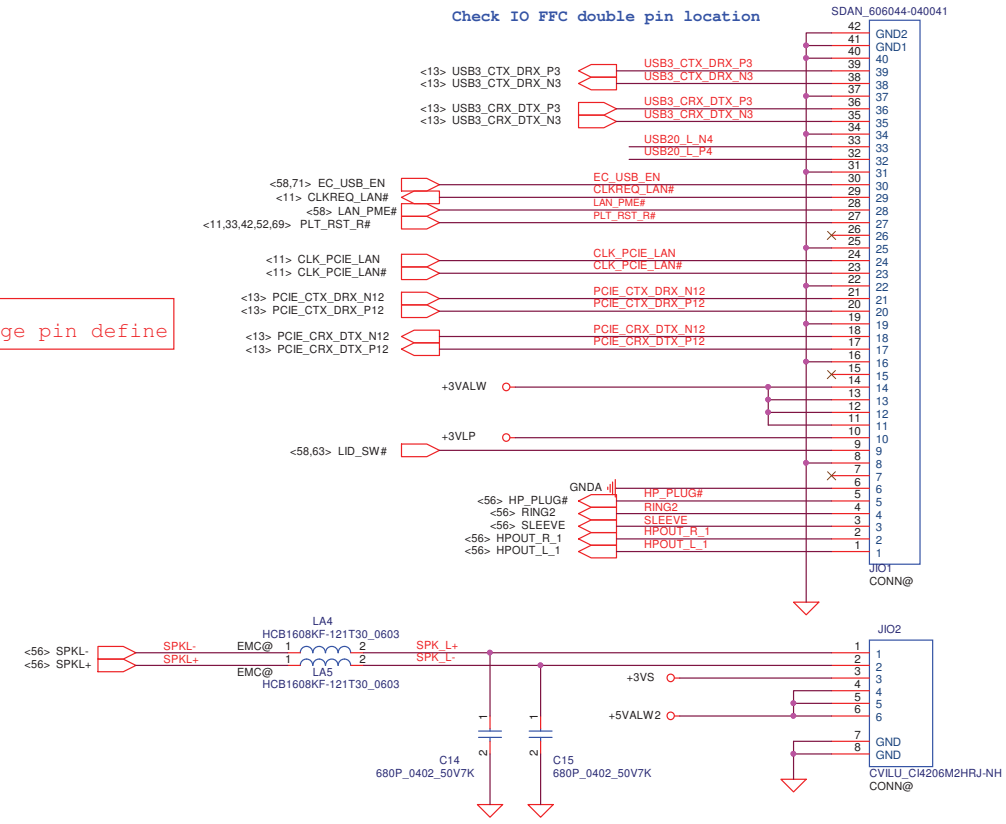
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IO/B CONN



0603  
- IO\_B change pin define



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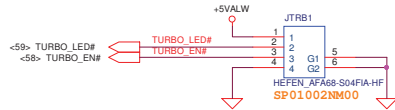
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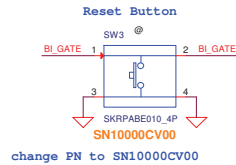
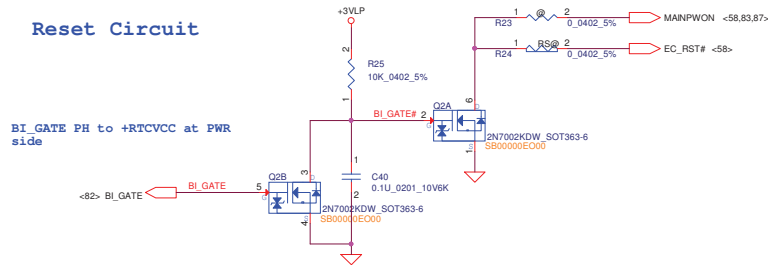
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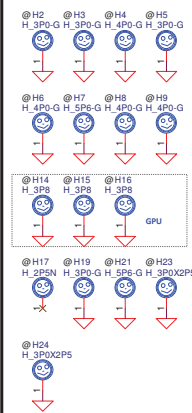
## Turbo Key



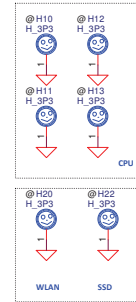
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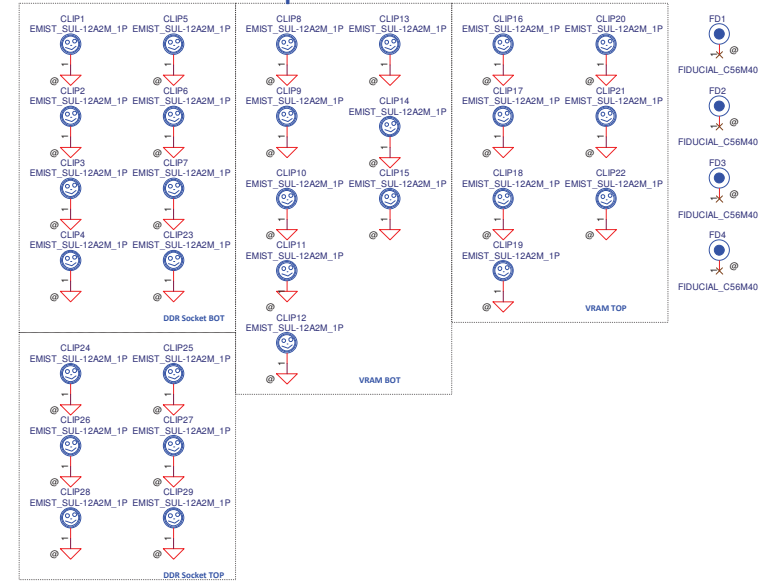
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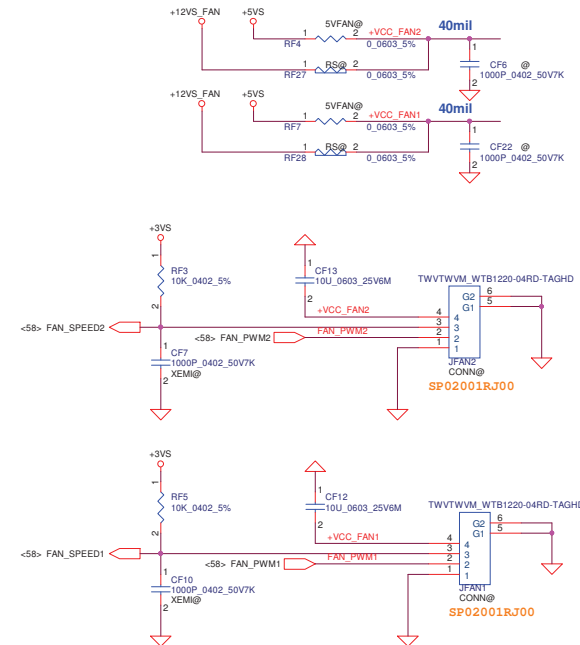
## Stand OFF



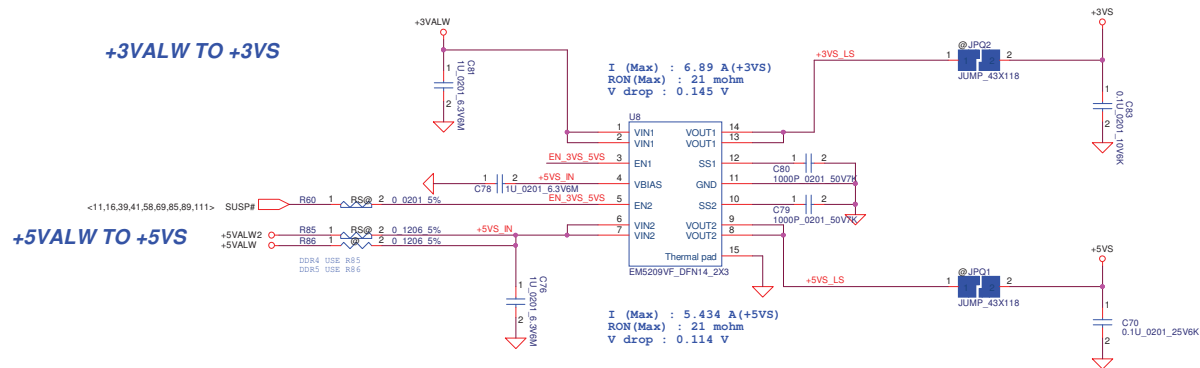
## Clips



## FAN Conn



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20210610  
- Move +1.8VALW to +1.8VS to page 69

20200717  
- Remove VGA Power sequence

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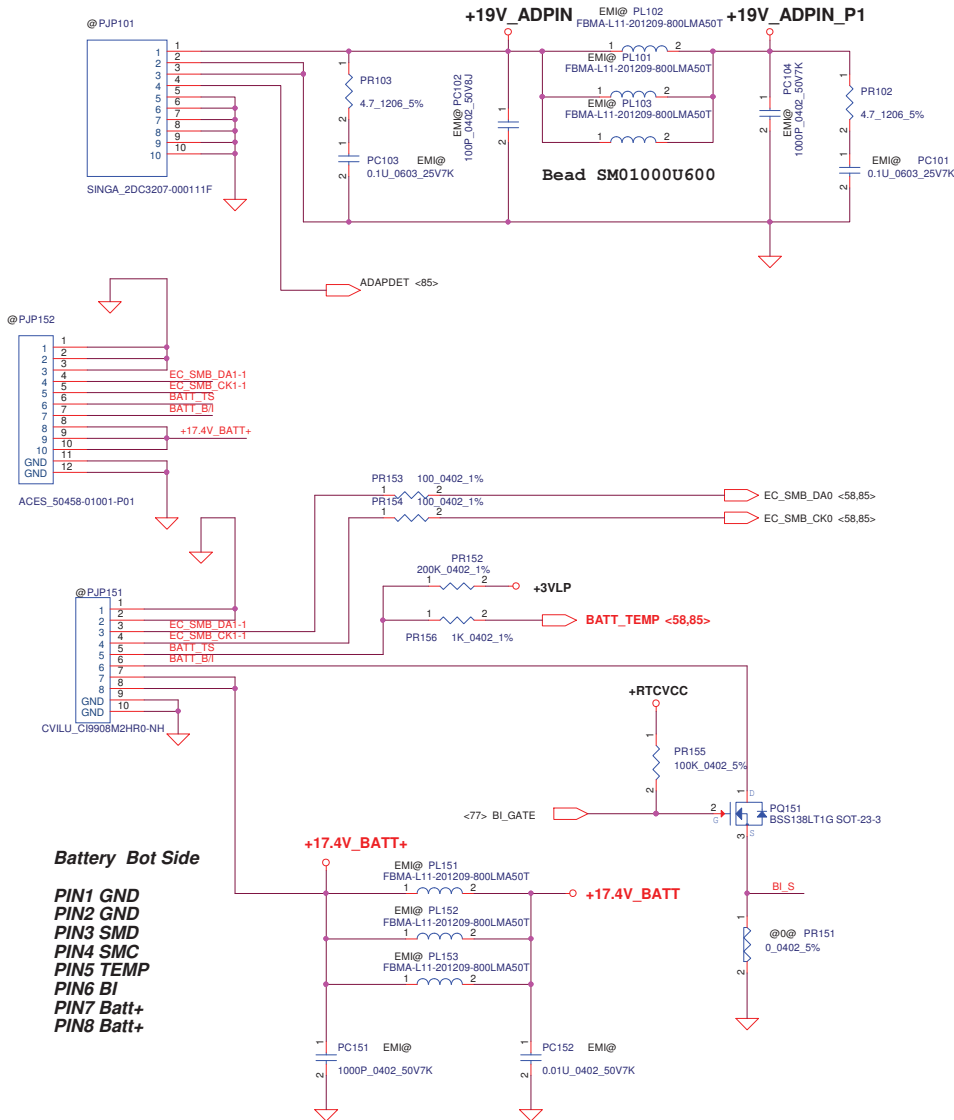
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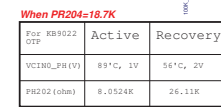
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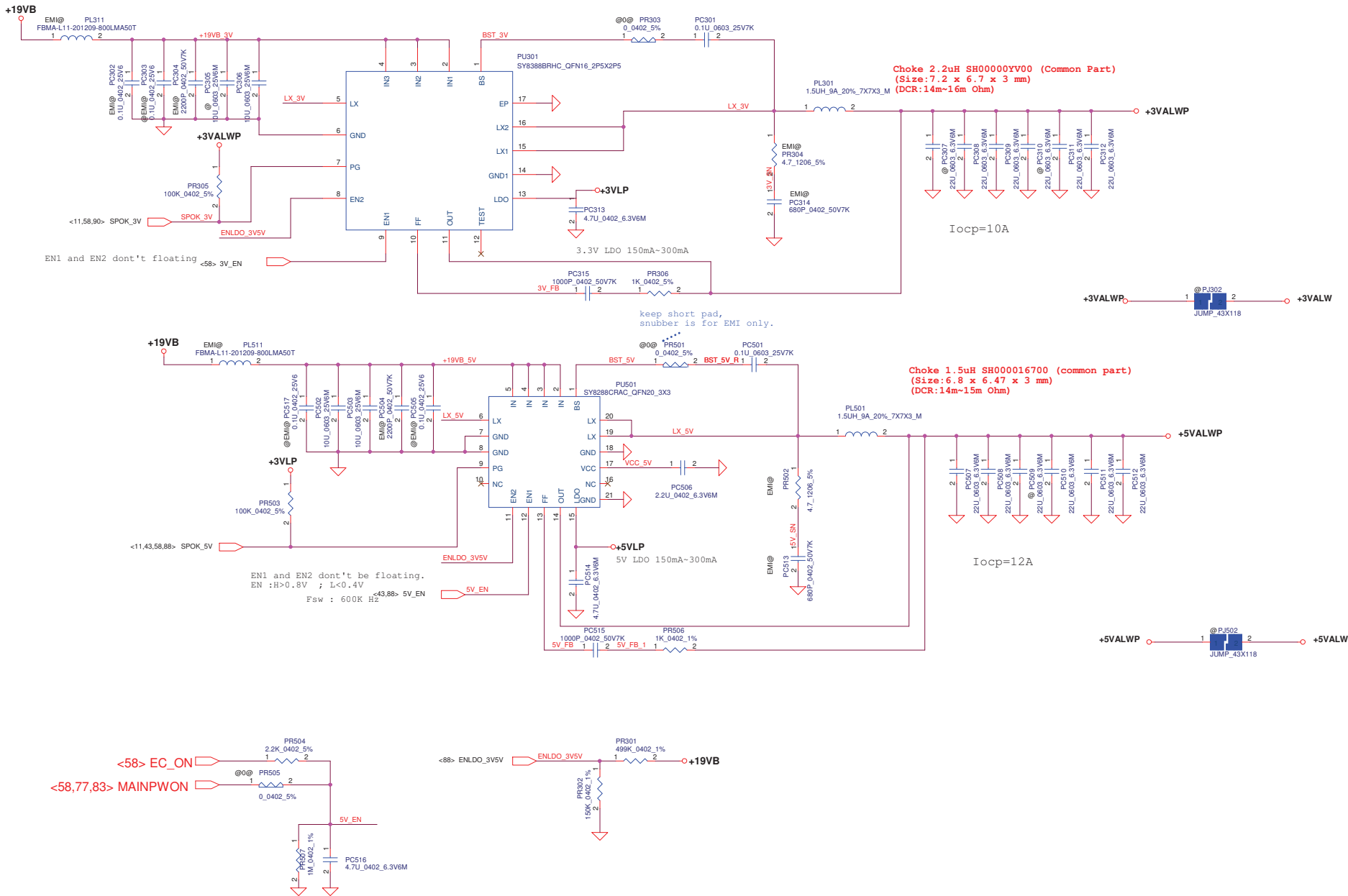
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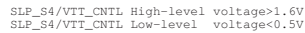
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```
Module model information
TPS51486_V1.mdd
```



**Table 1. VTT\_CNTL and SLP\_S4 Control for Output State**

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)



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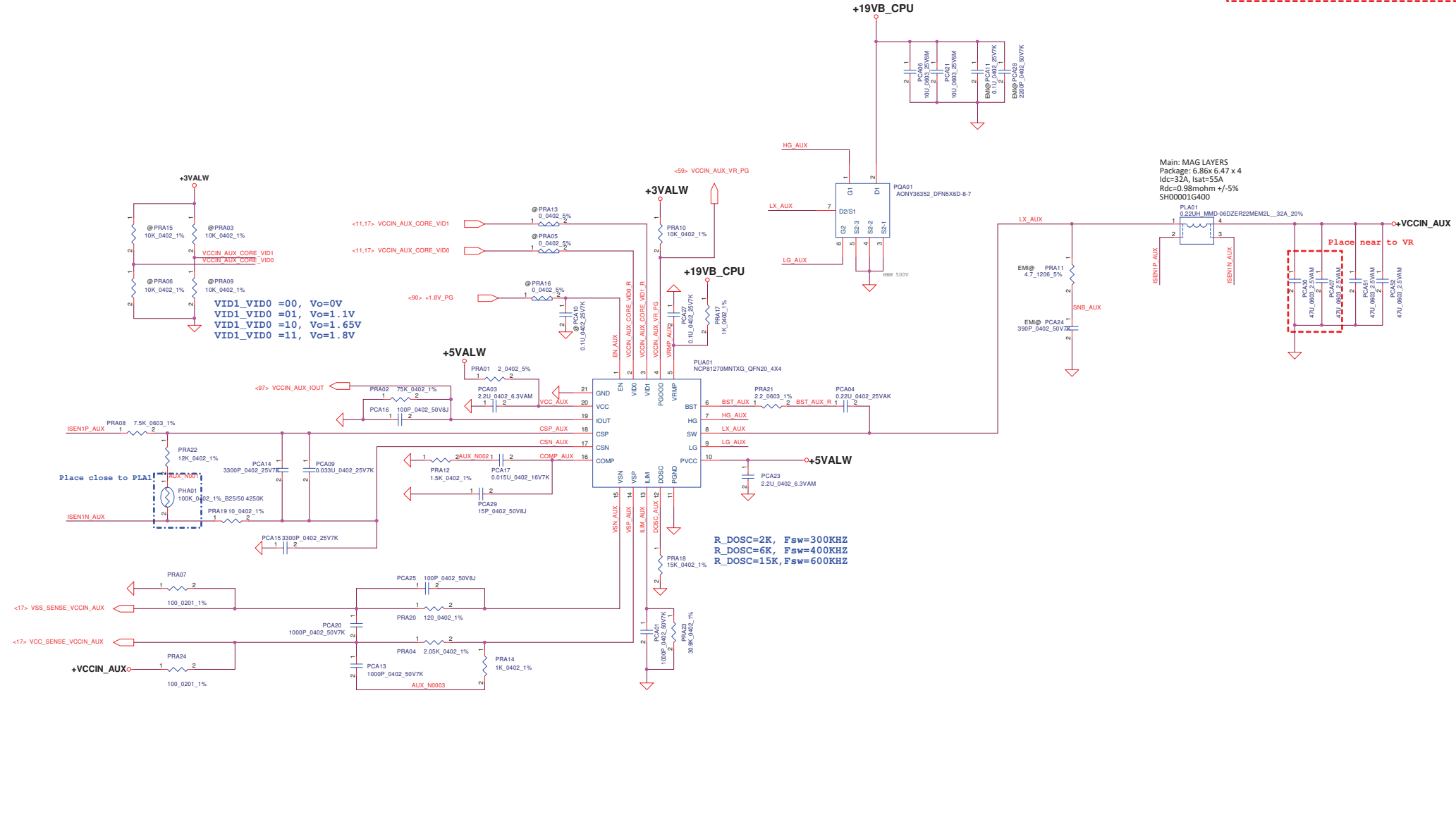
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Main Func = +VCCIN\_AUX

+VCCIN\_AUX  
Vout 1.8V  
IPL2(TDC) = 17A  
Peak Current = 34.2A(ICCmax)  
OCP: 44.6 A  
OVP: VID+0.36V (max 2V)  
FSW= 600KHz



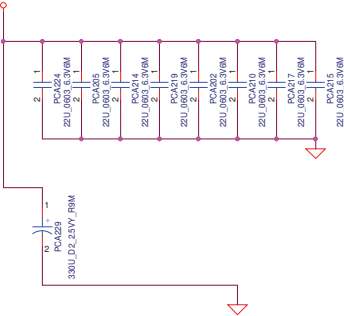
Main: MAG LAYERS  
Package: 6.86x 6.47 x 4  
I<sub>dc</sub>=32A, I<sub>sat</sub>=55A  
R<sub>dc</sub>=0.98mohm +/-5%  
SH00001G400

PLA01  
0.22UH MMD-0RDZER22MEN2L\_32A\_20%

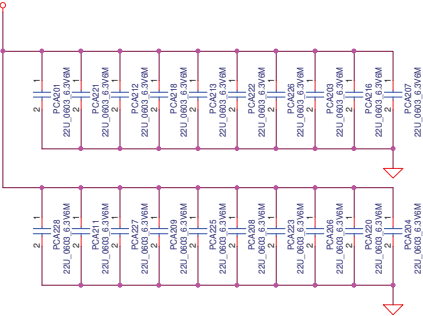
Place near to VR

R\_DOSC=2K, Fsw=300KHz  
R\_DOSC=6K, Fsw=400KHz  
R\_DOSC=15K, Fsw=600KHz

CPU Primary Side  
+VCCIN\_AUX



CPU Secondary side  
+VCCIN\_AUX

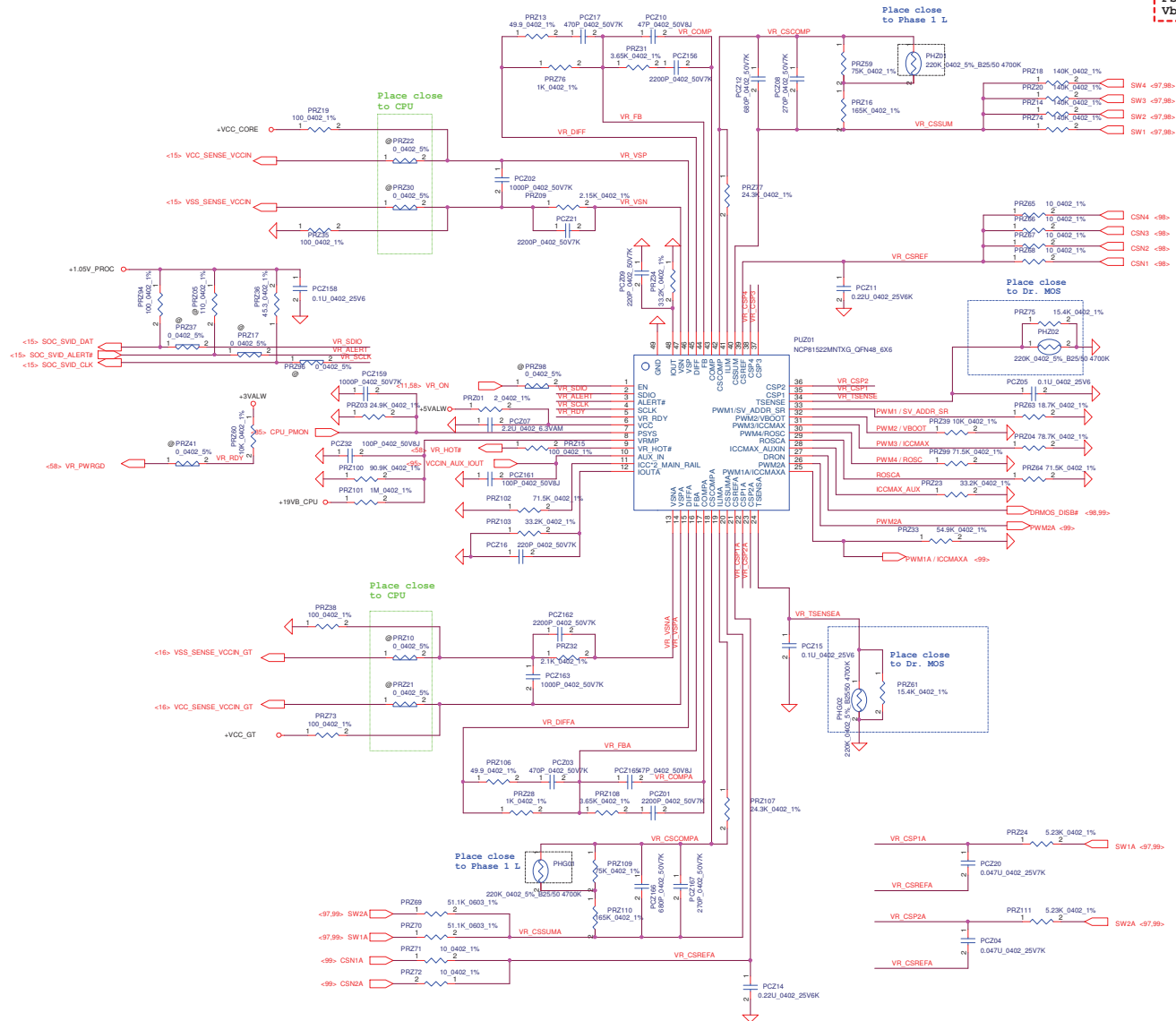




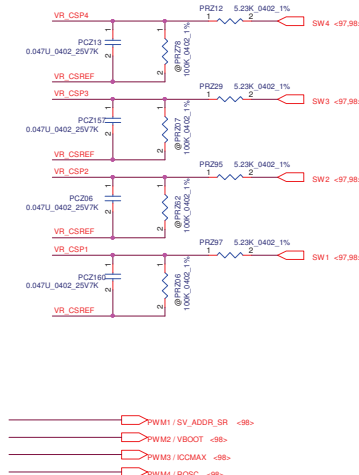
Main Func = CPU (IA/GT)

```
+VCC_CORE
IPL2 = 93A
Peak Current = 160A(ICCmax)
DC Load line: 2.1mohm
AC Load line: 2.1mohm
Current limit =200A(OCp)
OVP: VID+0.36V
FSW= 540K Hz
Vboot: 0V
```

```
+VCC_GT
IPL2 = 30A
Peak Curren = 50A(ICCmax)
DC Load line: 3.1mohm
AC Load line: 3.1ohm
Current limit =65A(OCp)
OVP: VID+0.36V
FSW= 540K Hz
Vboot: 0V
```



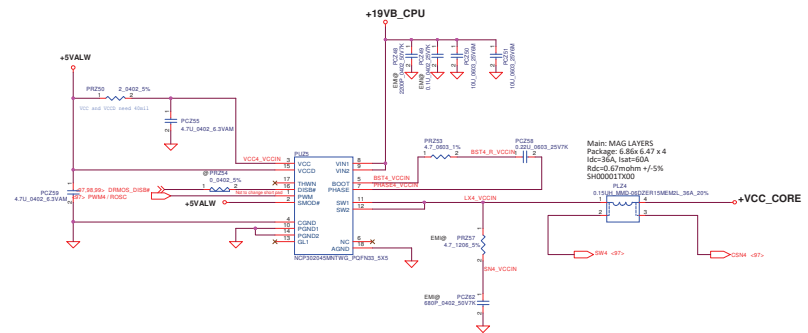
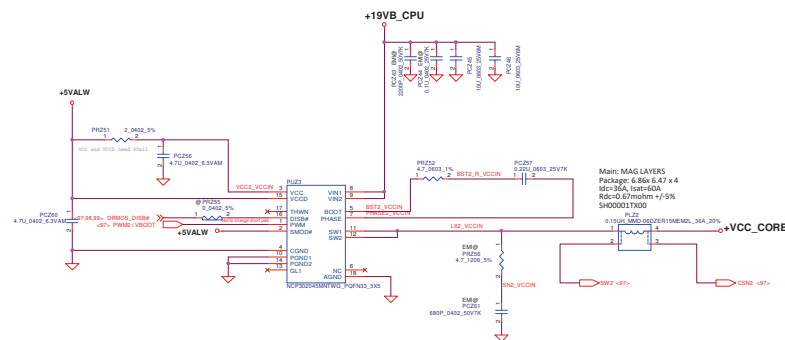
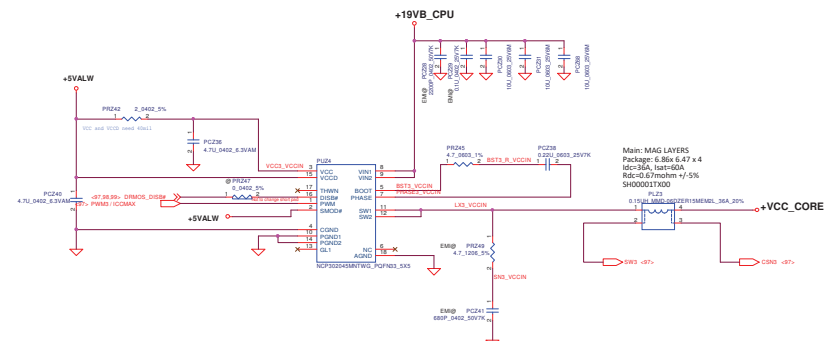
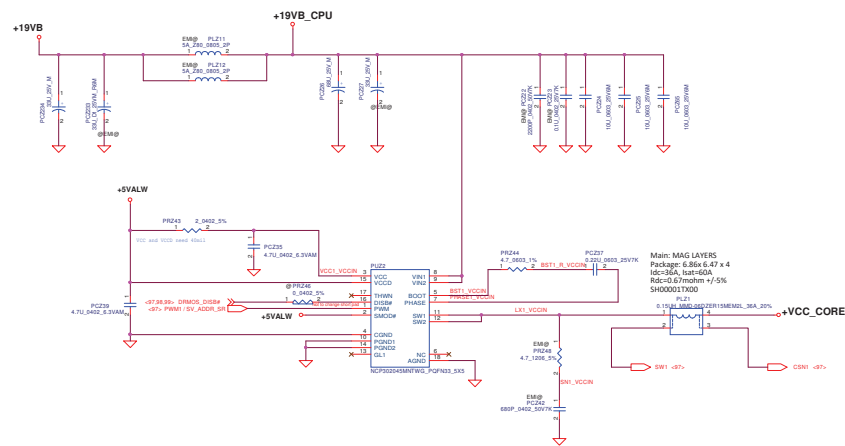
## PHASE DETECTION



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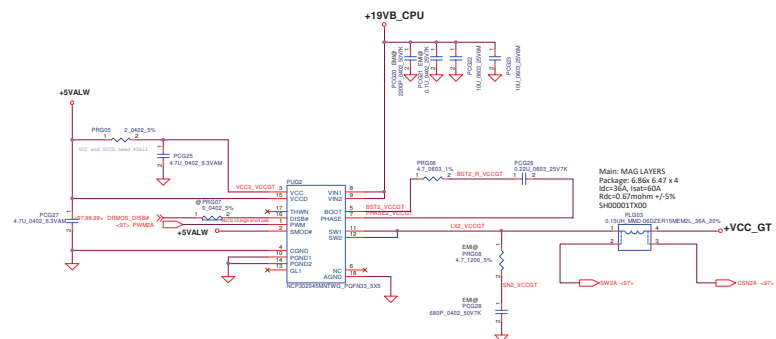
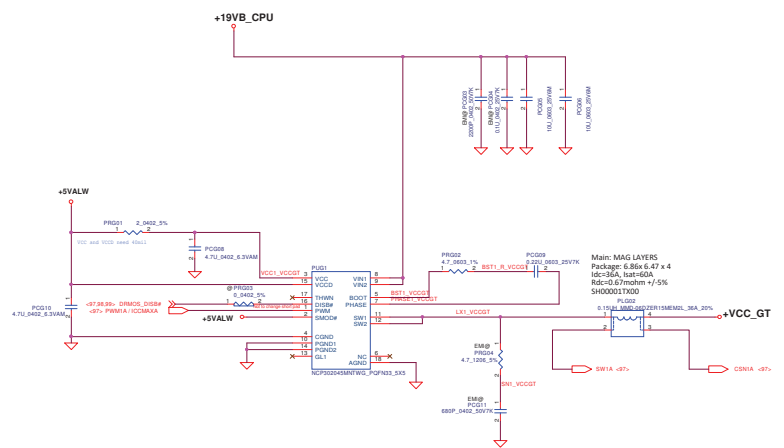
Main Func = +VCCCORE

+VCCCORE  
IPL2 = 93A  
Peak Curren = 160A(I0Cmax)  
DC Load line: 2.1mohm  
AC Load line: 2.1mohm  
Current limit ->A(OCP)  
FSW= K Hz



Main Func = +VCCGT

```
+VCCGT
IPL2 = 30A
Peak Current = 50A(ICCmax)
DC Load line: 3.1mohm
AC Load line: 3.1ohm
Current limit =A(OCp)
FSW= K Hz
```



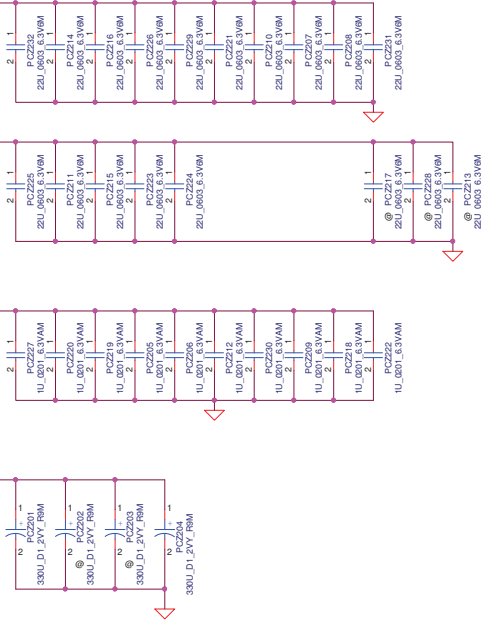
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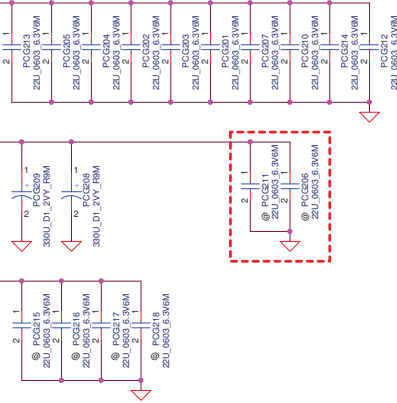
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Main Func = +VCCIN DECOUPLING

+VCC\_CORE



+VCC\_GT



Compal  
+VCCGT Output CAP :

CPU primary side:  
330uF\_B2 \*3pcs  
22uF\_0603\_low-noise \*16pcs

CPU Secondary side:  
22uF\_0603\_low-noise \*7pcs

Compal(follow PDG)  
+VCC\_GT Output CAP :

CPU Primary Side:  
330uF\_B2 \*3pcs  
47uF\_0603\_low-noise \*7 pcs  
22uF\_0603\_low-noise \*2 pcs

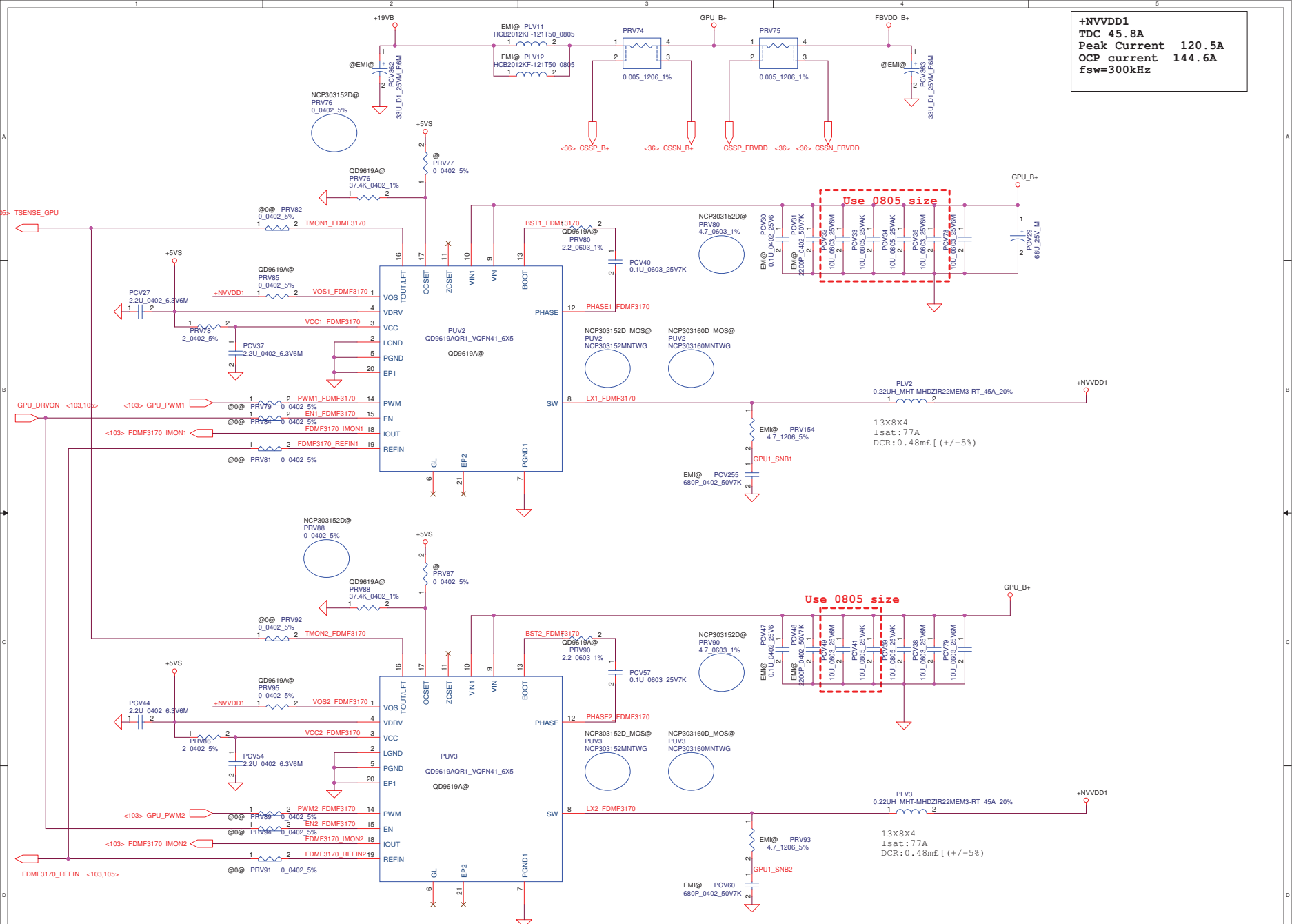
CPU Secondary side:  
22uF\_0603\_low-noise \*6 pcs  
10uF\_0603\_low-noise \*2 pcs

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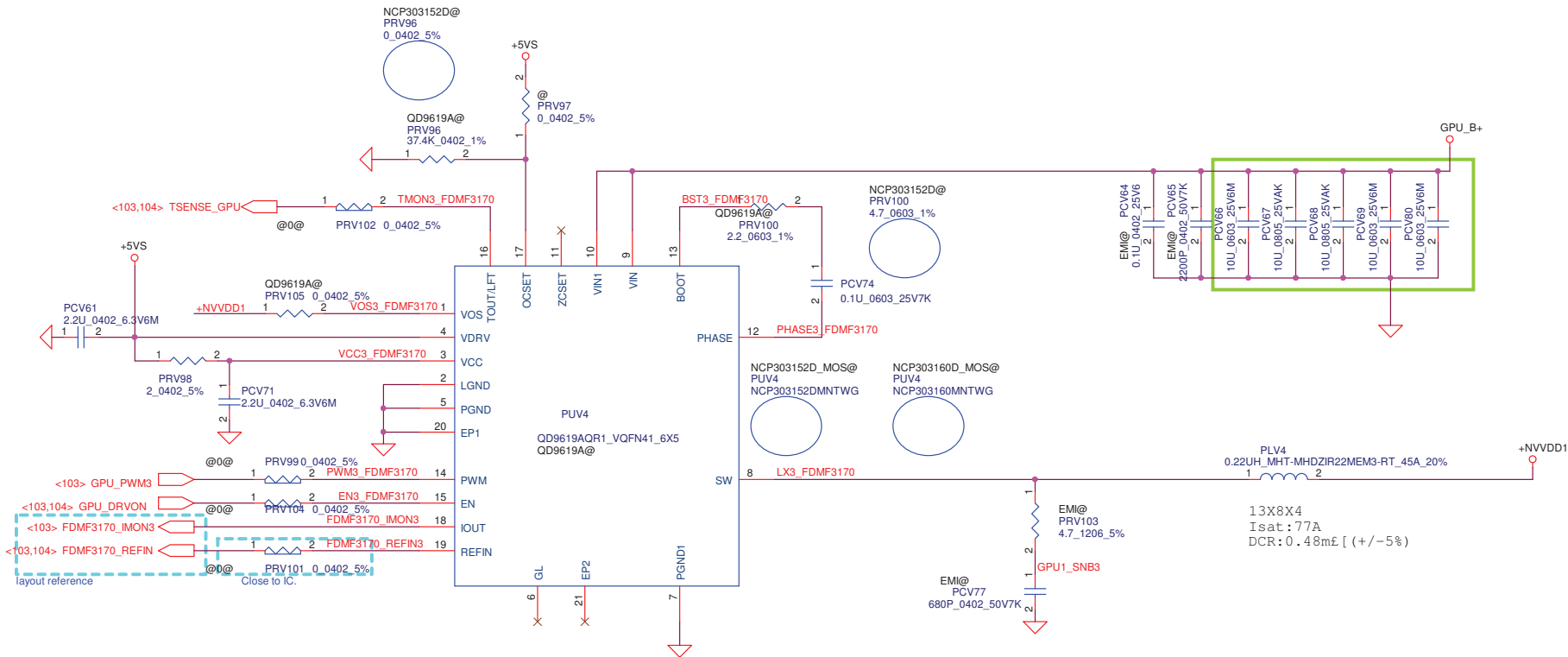


+NVVDD1  
TDC 45.8A  
Peak Current 120.5A  
OCP current 144.6A  
fsw=300kHz



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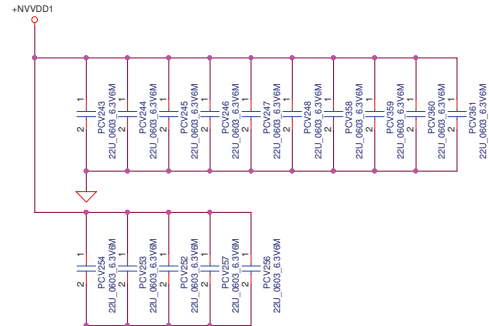
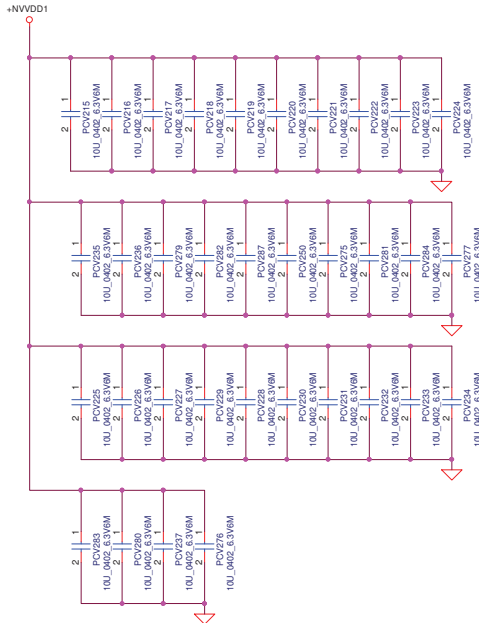
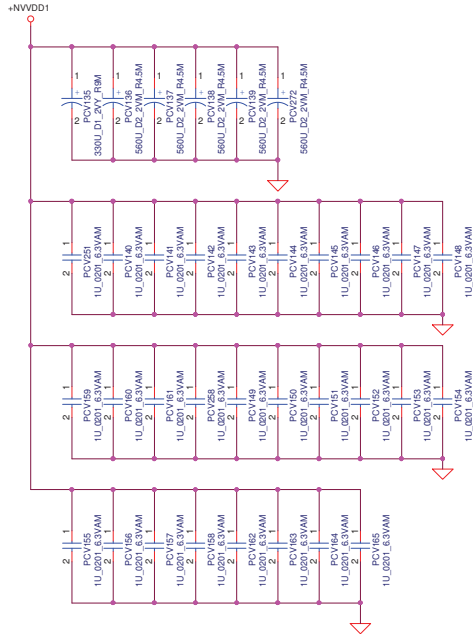


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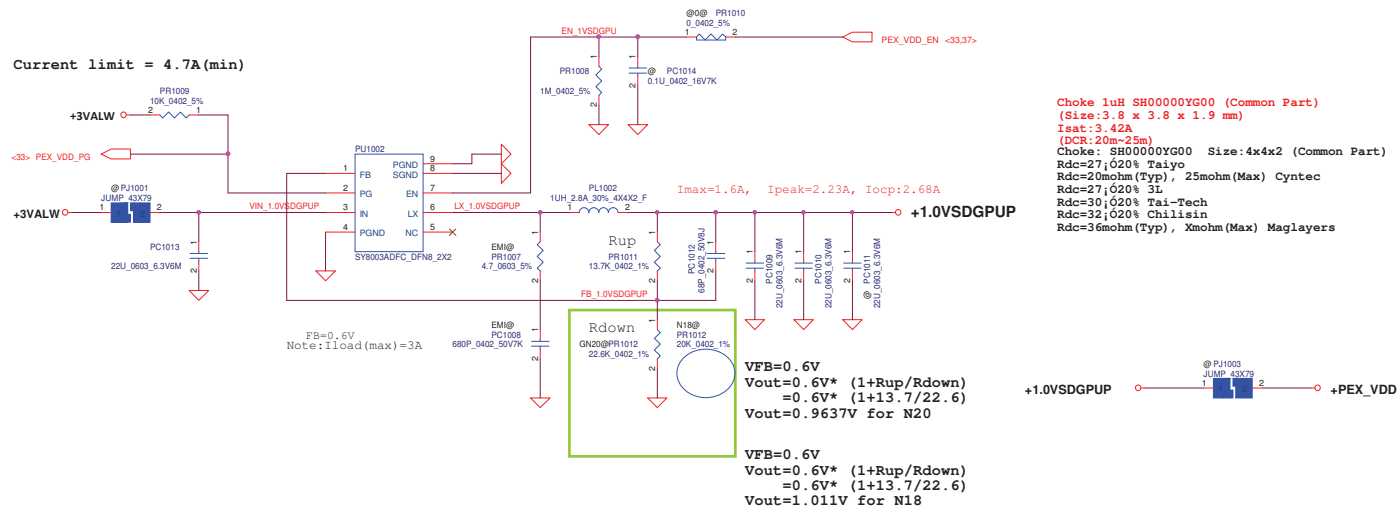
+NVVDD  
560uF X 6  
22uF\_0603 X 15  
10uF\_0402X 34  
1uF\_0201 X 28

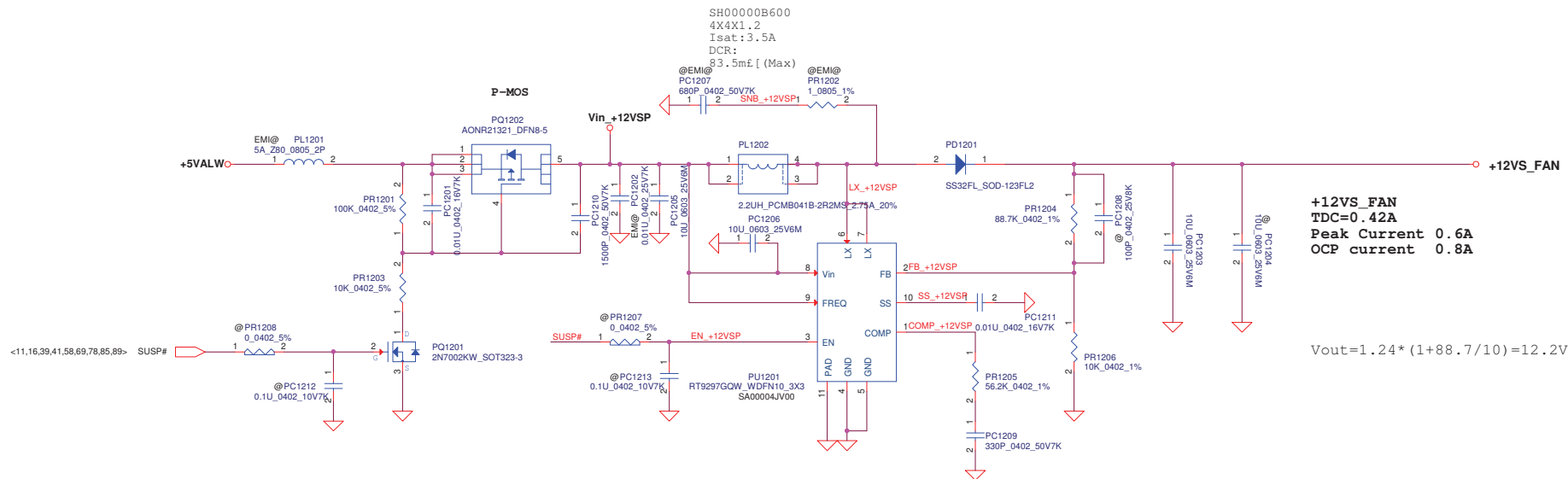




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